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This journal records developments in the application of electronics in science, industry, and the home. It contains information on the properties and performance of solid-state devices, valves and tubes, and associated components and assemblies. The practical circuits given are designed to provide the best working conditions and performance for the devices used. The design principles may be used (so far as device ratings allow) for adaptation to meet particular requirements. Current data should be consulted before any circuit is considered for production. Mullard Limited can normally supply only those devices or assemblies listed in the Company's current catalogues. Availability in quantity should be confirmed.

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The influence of adjuster mechanisms on the temperature coefficients of ferrite-core assemblies

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The contribution of the adjuster mechanism to the temperature coefficient of inductance of ferrite-cored inductor assemblies is discussed. Two different designs, the stud-type and nut-type, are distinguished and their temperature behaviours are compared. It is shown that the stud-type adjuster increases the temperature coefficient of inductance by a small amount, as expected, whereas the nut-type adjuster decreases it by an appreciable amount. The actual reduction is unpredictable since it is a complicated function of the adjuster position.

INTRODUCTION

A previous article described the adjuster developed for the Mullard RM-series of ferrite inductor cores and briefly considered the contribution of the adjuster to the temperature coefficient of a complete core assembly (Ref. 1). With the demand for inductor cores having narrower temperature coefficient limits, it is becoming increasingly important to know exactly the contribution of the adjuster mechanism to the temperature coefficient of the assembly. This particular aspect of adjuster performance is described in this article.

It is well known that the temperature coefficient α_L of a gapped inductor is given by:

$$\alpha_L = \mu_e \alpha_{Fc}\,, \qquad \ldots(1)$$

where μ_e is the effective permeability of the gapped ferrite core and α_{Fc} is the temperature factor of the ferrite core material. In practice, the manufacturer states the limits of the effective permeability of the core without an adjuster, designated μ_e', and controls the value of α_{Fc} within certain limits. The adjuster is then used to raise the effective permeability of the assembly to a value μ_e which gives the required inductance or resonant frequency. It is this nominal value of μ_e, corresponding approximately to the mid-range position of the adjuster, that is used by the inductor designer to calculate the performance of the core; that is, the inductance, the limits of temperature coefficient, etc.

Because the adjuster increases the effective permeability of the core, the temperature coefficient would be expected to increase according to Eq. 1. Indeed, if the adjuster were perfect, making no contribution to the temperature coefficient of the inductor, Eq. 1 would be obeyed. In such a case, with the assembly adjusted to nominal μ_e, the temperature coefficient limits would be as calculated from the nominal value of μ_e irrespective of the physical position of the adjuster. In practice, however, there are factors that may cause departures from the ideal and some of these are considered below.

INFLUENCE OF ADJUSTER TUBE MATERIAL

The following expression for the temperature coefficient of a ferrite core with adjuster has been derived using an equivalent magnetic circuit.

$$\alpha_L = \frac{LR_c}{N^2}(\alpha_{\mu c} + K\alpha_{\mu t}), \qquad \ldots(2)$$

where

$\alpha_{\mu c}$ is the temperature coefficient of the core material,
$\alpha_{\mu t}$ is the temperature coefficient of the adjuster tube material,
L is the inductance of the gapped core with adjuster,
R_c is the reluctance of the ungapped core,
N is the number of turns,
K is a constant for a particular gapped core which depends on the position of the adjuster.

Eq. 2 can be rewritten:

$$\alpha_L = \frac{LR_c}{N^2}(\alpha_{Fc}\mu_c + K\alpha_{Ft}\mu_t),$$

where

α_{Fc} is the temperature factor of the core material,
α_{Ft} is the temperature factor of the adjuster tube material,
μ_c is the permeability of the core material,
μ_t is the permeability of the adjuster tube material.

From Eq. 2 also:

$$\alpha_L = \frac{\mu_e}{\mu_c}(\alpha_{Fc}\mu_c + K\alpha_{Ft}\mu_t),$$

and, if $\mu_c = \mu_t$:

$$\alpha_L = \mu_e(\alpha_{Fc} + K\alpha_{Ft}). \qquad \ldots(3)$$

For the special case where $\alpha_{Fc} = \alpha_{Ft}$:

$$\alpha_L = \mu_e \alpha_{Fc}(1 + K), \qquad \ldots(4)$$

and with no adjuster present Eq. 4 becomes:

$$\alpha_L = \mu_e \alpha_{Fc},$$

which is the same as Eq. 1.

Typical values of K for 25mm Vinkors with the adjuster in the maximum inductance position, that is symmetrically across the air gap, are given in Table 1.

TABLE 1
Values of K for 25mm Vinkors with the adjuster in the maximum inductance position

Core Assembly	Adjuster	μ_e'	μ_e	Adjustment range $\frac{\Delta L}{L}$(%)	K
LA1414	LA1340	59·1	63	13	0·153
LA1221	LA1275	90·1	100	22	0·081
LA1220	LA1275	145	160	20	0·029
LA1219*	LA1275	236·5	250	11	0·008

*The adjustment range of the LA1219 assembly is 15% with the extended range adjuster type LA1266.

Using the equations already derived and the values of K in Table 1, it is possible to calculate the contribution of the adjuster to the assembly temperature coefficient. In Table 2, the effects of variations in both α_{Fc} and α_{Ft} are calculated for an LA1221, $\mu_e = 100$, Vinkor assembly. The limits of α_{Fc} and α_{Ft} are taken as $0{\cdot}5\times10^{-6}$/degC and $1{\cdot}5\times10^{-6}$/degC which represent worst-case conditions.

TABLE 2
Calculated effects of variations in α_{Ft} and α_{Fc} on the temperature coefficient of an LA1221 assembly

Example	α_{Fc} ($\times10^{-6}$/degC)	α_{Ft} ($\times10^{-6}$/degC)	Temperature coefficient with adjuster (ppm/degC)	
			minimum position	maximum position
1	0·5	0	45	55
2	0·5	0·5	45	59
3	0·5	1·5	45	68
4	1·5	0	135	165
5	1·5	0·5	135	169
6	1·5	1·5	135	178

In Table 2, examples 1 and 4 are equivalent to ignoring the effects of the adjuster tube temperature coefficient and using Eq. 1. Also, the minimum position corresponds to the assembly without an adjuster.

Several important conclusions can be drawn from these formulae and calculations.

1) The simple relationship $\alpha_L = \mu_e\alpha_{Fc}$ underestimates the contribution of the adjuster to the assembly temperature coefficient.
2) The contribution of the adjuster to the assembly temperature coefficient is dependent on the temperature factor of the adjuster tube material α_{Ft}.
3) The contribution of the adjuster to the assembly temperature coefficient, expressed as a percentage increase, is most significant where the temperature factor of the core material α_{Fc} is at its lower limit ($0{\cdot}5\times10^{-6}$/degC).
4) The contribution of the adjuster to the assembly temperature coefficient is larger on cores with low μ_e because of the higher value of K.
5) If a batch of assemblies is measured with and without adjusters, there will inevitably be a greater spread in the range of temperature coefficients when the adjusters are inserted.

ADJUSTER DESIGN

Before analysing temperature coefficient measurements on inductor assemblies complete with adjusters, it is necessary to recognize two types of screw thread adjuster, the stud type and the nut type. In the stud-type adjuster, shown in Fig. 1, the ferrite tube is moulded to a plastic carrier which has a central hole concentric with the ferrite tube. In the Mullard design, the cross section of this central hole is approximately an equilateral triangle. As the adjuster is screwed on to the threaded brass stud, a thread is impressed into the three flats of the central hole by the screwing action. In this way, the adjuster is made self-locking and vibration-proof, and is relatively free from backlash. The ferrite tube is supported almost directly by the threaded stud and hence its axial position is largely controlled by the dimensional stability of this stud and not by the plastic carrier. The design of the Mullard RM-core skirted-head adjuster, shown in Fig. 1, and that of the Vinkor adjuster with three ribs*, ensure that the adjuster head does not affect the contribution of the adjuster mechanism to the assembly temperature coefficient. All Mullard adjusters with the exception of those intended for 10 and 12mm Vinkors are stud-type adjusters.

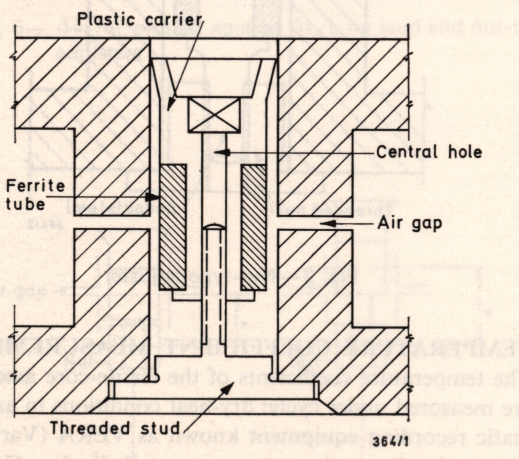

Fig. 1—Stud-type adjuster

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*To be replaced shortly by the RM-core skirted type.

The nut-type adjuster shown in Fig. 2 has a shank (or stem) which is an extension of the plastic carrier beyond the ferrite tube. This shank, which may be plain or threaded, is screwed into a threaded nut. In the design shown in Fig. 2 the stability of the axial position of the adjuster tube is dependent on the dimensional stability of the shank. A nut-type adjuster with a plain square-section shank is used in 10 and 12mm Vinkors. On screwing the adjuster into the threaded nut, a thread is impressed on the four corners of the shank. In another design of nut-type adjuster in common use, a round shank with a pre-formed thread engages, within dimensional tolerances, with the thread of the nut.

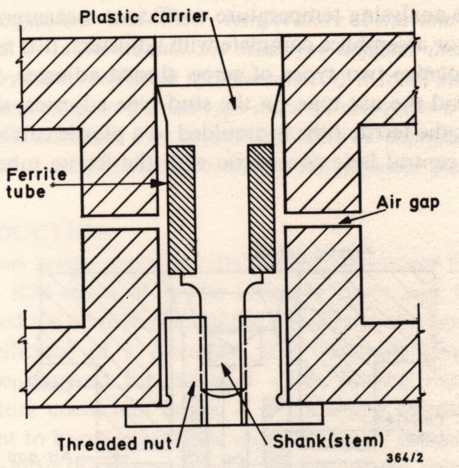

Fig. 2—Nut-type adjuster

TEMPERATURE COEFFICIENT MEASUREMENTS

The temperature coefficients of the ferrite-core assemblies are measured under cyclic dry-heat conditions in an automatic recording equipment known as VERA (Variability Electronic Recording Apparatus, Ref. 2). Carefully aligned, cemented assemblies are used as test beds. These assemblies without adjusters are first cycled between +30 and +70°C until their inductance drifts are negligible. The adjusters are then inserted at the 30°C temperature level without disturbing the temperature cycle and, after a minimum of five cycles, the temperature coefficients are measured. The position of the adjusters for each measurement is set by using the VERA oscillator and frequency counter, having previously calculated the resonant frequencies corresponding to the required position of each adjuster. The results of measurements on five stud-type adjusters are shown in Fig. 3, and on five nut-type adjusters, in Fig. 4.

It is apparent from Figs. 3 and 4 that the two basic types of screw-thread adjuster have different characteristics; the nut-type adjuster also shows a greater variance.

In Fig. 5 the averaged results of Figs. 3 and 4 are plotted as the percentage change of temperature coefficient $\Delta\alpha_L/\alpha_L$ against the percentage change of inductance $\Delta L/L$ caused by insertion of the adjuster. Fig. 5 also shows the 'ideal' curve; that is, the one in which $\Delta\alpha_L/\alpha_L$ is proportioned to $\Delta L/L$. For an ideal adjuster, the contribution of the adjuster mechanism to the temperature coefficient of the assembly is zero. The stud-type adjuster is seen to approach the ideal curve more closely than the nut-type adjuster. However, the nut-type adjuster significantly reduces the assembly temperature coefficient. Since the degree of this reduction depends on the adjuster position which in practice might be anywhere within the adjustment range, the final temperature coefficient of the assembly is unpredictable within wide limits.

The reduction in assembly temperature coefficient for the nut-type adjuster can be explained by the thermal expansion of the plastic shank, as shown in Fig. 6. The effective length l_e of the adjuster increases with temperature because of thermal expansion. It also increases as the adjuster is screwed out. Hence, when the adjuster is screwed fully in and the inductance is a maximum, l_e is a minimum and the effect on the assembly temperature coefficient is also a minimum. When the adjuster is screwed out to a position near minimum inductance, l_e is a maximum and the effect on the assembly temperature coefficient is greatest. It can be shown that the linear thermal expansion of the plastic shank, typically 15μm for a 40degC temperature change on an RM6 adjuster, produces an axial movement of the adjuster tube which reduces the inductance by an amount corresponding to the lower temperature coefficient observed. Similar results on nut-type adjusters have also been observed elsewhere (Ref. 3).

In summarizing the results of the measurements, the following points emerge.

1) The stud-type adjuster, which includes all Mullard adjusters with the exception of those used in the 10 and 12mm Vinkors, increases the assembly temperature coefficient almost in proportion to the increase of μ_e due to insertion of the adjuster. This type of adjuster is therefore suitable for assemblies with narrow temperature coefficient limits.

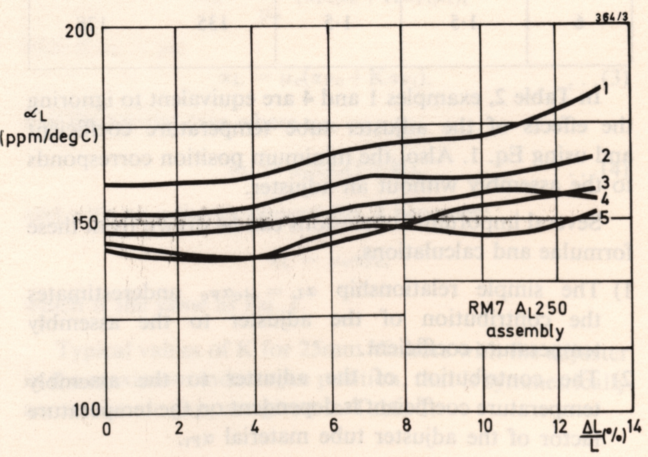

Fig. 3—α_L plotted against $\Delta L/L$ for RM7 core assemblies with stud-type adjusters

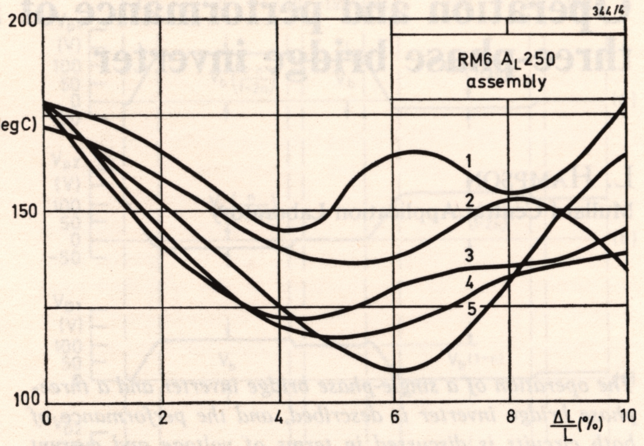

Fig. 4—α_L plotted against $\Delta L/L$ for RM6 core assemblies with nut-type adjusters

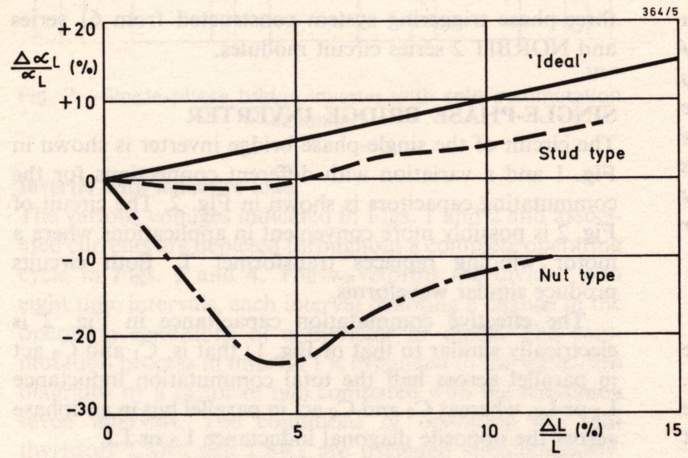

Fig. 5—$\Delta\alpha_L/\alpha_L$ plotted against $\Delta L/L$ for stud and nut-type adjusters

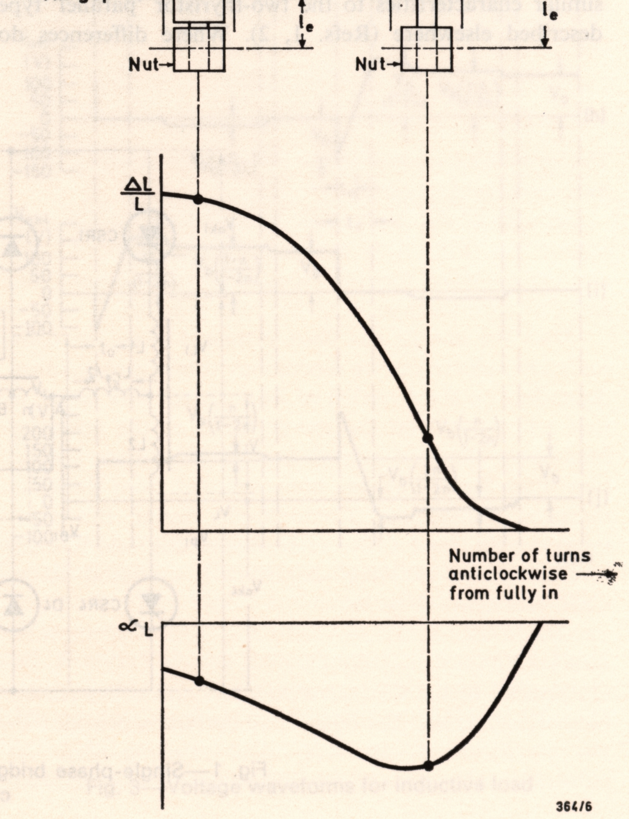

Fig. 6—Effects of temperature changes on nut-type adjusters (right)

2) The nut-type adjuster reduces the assembly temperature coefficient by a significant amount. However, this is unpredictable since it depends on the position of the adjuster and cannot be compensated. This type of adjuster therefore has limitations when used in applications requiring narrow temperature coefficient limits, for example direct modulation channel filter coils and oscillator circuit coils.

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Operation and performance of a single-phase and a three-phase bridge inverter

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UDC 621.314.58:621.382.333.4

The operation of a single-phase bridge inverter and a three-phase bridge inverter is described, and the performance of both circuits is discussed in terms of voltage and current waveforms for reactive and resistive loads. Selection of the required commutation capacitance and inductance values is also described. For the three-phase inverter, the method of ensuring correct phase rotation is described and waveforms are given showing the relationship between the phases of the supply and the commutation sequence. Finally, details are given of a three-phase thyristor trigger circuit which is constructed from 61 series and NORBIT 2 series circuit modules. The circuit is capable of phase rotation in either direction.

INTRODUCTION

This article describes the performance of bridge-type inverters for both single-phase and three-phase operation. In general, the bridge inverter is operated in the mode known as forced commutation, and the resultant output waveform is squarewave. In this respect, it has many similar characteristics to the two-thyristor 'parallel' type described elsewhere (Refs. 1, 2). Where differences do exist, they lie in the different magnitudes of voltages and component values rather than in the principle of operation.

In addition to describing single-phase and three-phase inverter operation, the article also contains details of a three-phase triggering system constructed from 61 series and NORBIT 2 series circuit modules.

SINGLE-PHASE BRIDGE INVERTER

The circuit of the single-phase bridge inverter is shown in Fig. 1 and a variation with different connections for the commutating capacitors is shown in Fig. 2. The circuit of Fig. 2 is possibly more convenient in applications where a motor winding replaces transformer T. Both circuits produce similar waveforms.

The effective commutation capacitance in Fig. 2 is electrically similar to that of Fig. 1; that is, C_1 and C_4 act in parallel across half the total commutation inductance L_1 or L_2, whereas C_3 and C_2 act in parallel but in antiphase across the opposite diagonal inductance L_3 or L_4.

The commutation capacitance in both circuits is also directly related in terms of VA ratings to the value required in the two-thyristor inverter circuit described in Refs. 1, 2.

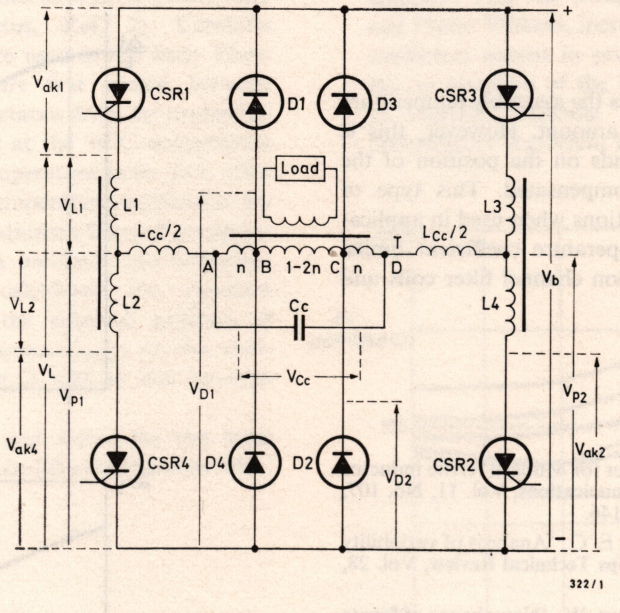


Fig. 1—Single-phase bridge inverter with one commutation capacitor

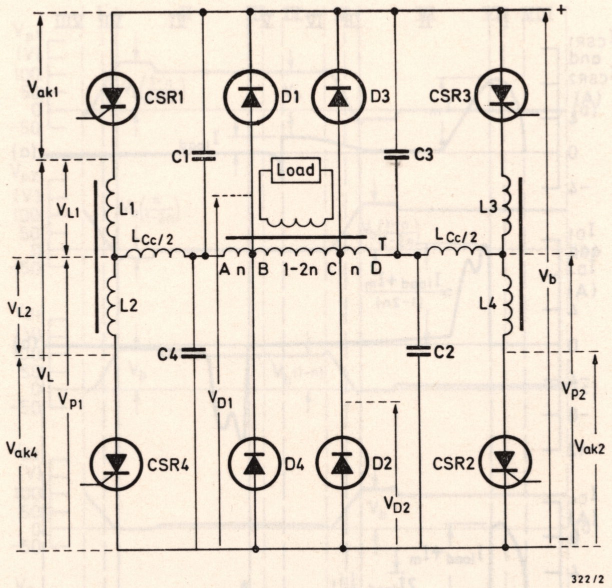


Fig. 2—Single-phase bridge inverter with split commutation capacitors

Inverter with inductive load

The various voltages indicated in Figs. 1 and 2 and associated currents are depicted throughout a complete operating cycle in Figs. 3 and 4. The waveforms are divided into eight time intervals, each interval denoting a change in the operating conditions of a thyristor or diode. The commutation process in interval I is expanded in the waveform diagrams by a factor of two compared with the remaining seven intervals. The conditions of operation are that thyristors CSR_1 and CSR_2 are triggered simultaneously, followed by CSR_3 and CSR_4. Diodes D_1 to D_4 are tapped into the transformer T with a tapping ratio n of about 0·15. This value has been shown previously to give a good compromise between recovery of energy from the commutation inductances L_1 and L_2, and the re-applied forward voltage to each non-conducting thyristor (Ref. 1). A nominal supply voltage of 120V was used with an operating frequency for the inverter of about 250Hz.

Interval I

The end of interval VIII is linked in time with the start of interval I. Thyristors CSR_3 and CSR_4, acting together, conduct a 'steady' load current I_{load}. The right-hand side of capacitor Cc in Fig. 1 is charged to V_b volts (Fig. 3e). In Fig. 2, C_1 and C_2 are charged to V_b volts. Diodes D_1 to D_4 are non-conducting.

Commutation is initiated by triggering CSR_1 and CSR_2 simultaneously. Thyristor CSR_1 then connects the 'cathode' end of L_1 to the supply V_b, and similarly CSR_2 connects L_4 to neutral. The charge on capacitor Cc in Fig. 1 and C_1 to C_4 in Fig. 2 cannot change instantaneously, and therefore a reverse voltage (V_{L2} in Fig. 3) appears at the 'anode' end of L_2, causing CSR_4 to cease conduction. Similarly a forward blocking voltage V_{L1} appears across L_3, causing CSR_3 to cease conduction.

To preserve conditions of equilibrium in the circuit, the load current I_{load} previously flowing in L_2 and L_3 is transferred to L_1 and L_4, the energy stored in the induct-

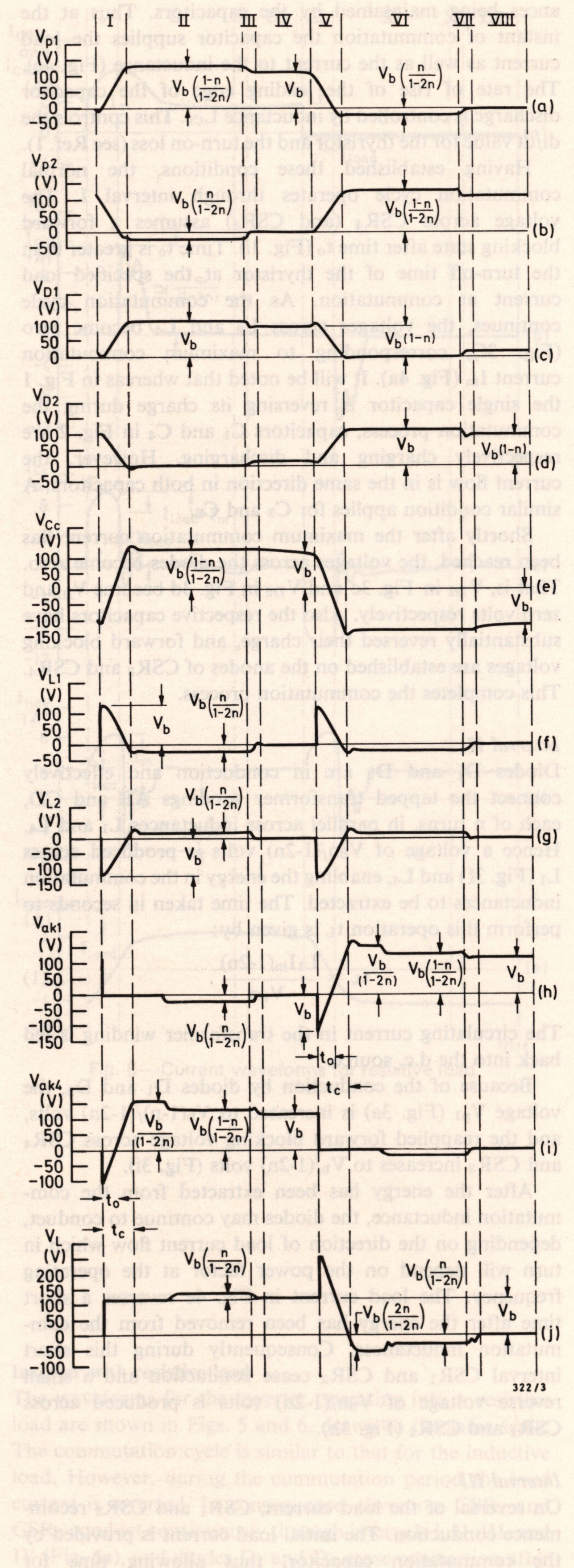


Fig. 3—Voltage waveforms for inductive load

ances being maintained by the capacitors. Thus at the instant of commutation the capacitor supplies the load current as well as the current to the inductance (Fig. 4c). The rate of rise of the leading edge of the capacitor discharge is controlled by inductance L_{Cc}. This controls the di/dt value for the thyristor and the turn-on loss (see Ref. 1).

Having established these conditions, the normal commutation cycle operates through interval I. The voltage across CSR_4 (and CSR_3) assumes a forward blocking state after time t_o (Fig. 3i). Time t_o is greater than the turn-off time of the thyristor at the specified load current at commutation. As the commutation cycle continues, the voltages across L_2 and L_4 become zero (Fig. 3f), corresponding to maximum commutation current I_m (Fig. 4a). It will be noted that whereas in Fig. 1 the single capacitor is reversing its charge during the commutation process, capacitors C_1 and C_4 in Fig. 2 are respectively charging and discharging. However, the current flow is in the same direction in both capacitors. A similar condition applies for C_3 and C_2.

Shortly after the maximum commutation current has been reached, the voltages across the diodes become zero. That is, V_{D1} in Fig. 3c and V_{D2} in Fig. 3d become V_b and zero volts respectively. Also the respective capacitors have substantially reversed their charge, and forward blocking voltages are established on the anodes of CSR_3 and CSR_4. This completes the commutation process.

Interval II

Diodes D_1 and D_2 are in conduction and effectively connect the tapped transformer windings AB and CD, each of n turns, in parallel across inductances L_1 and L_4. Hence a voltage of $V_b n/(1-2n)$ volts is produced across L_1 (Fig. 3f) and L_4, enabling the energy in the commutation inductances to be extracted. The time taken in seconds to perform this operation t_L is given by:

$$t_L = \frac{L_1 I_m (1-2n)}{V_b n} \,. \qquad \ldots(1)$$

The circulating current in the transformer winding is fed back into the d.c. source.

Because of the conduction by diodes D_1 and D_2, the voltage V_{p1} (Fig. 3a) is increased to $V_b(1-n)/(1-2n)$ volts, and the reapplied forward blocking voltage across CSR_4 and CSR_3 increases to $V_b/(1-2n)$ volts (Fig. 3i).

After the energy has been extracted from the commutation inductance, the diodes may continue to conduct, depending on the direction of load current flow which in turn will depend on the power factor at the operating frequency. The load current in Fig. 4e reverses a short time after the energy has been removed from the commutation inductances. Consequently during this short interval CSR_1 and CSR_2 cease conduction and a small reverse voltage of $V_b n/(1-2n)$ volts is produced across CSR_1 and CSR_2 (Fig. 3h).

Interval III

On reversal of the load current, CSR_1 and CSR_2 recommence conduction. The initial load current is provided by the commutation capacitor, thus allowing time for inductances L_1 and L_4 to adjust to the new current conditions. This causes a disturbance in the zero current condition of the commutation capacitor (Fig. 4c, point i_1).

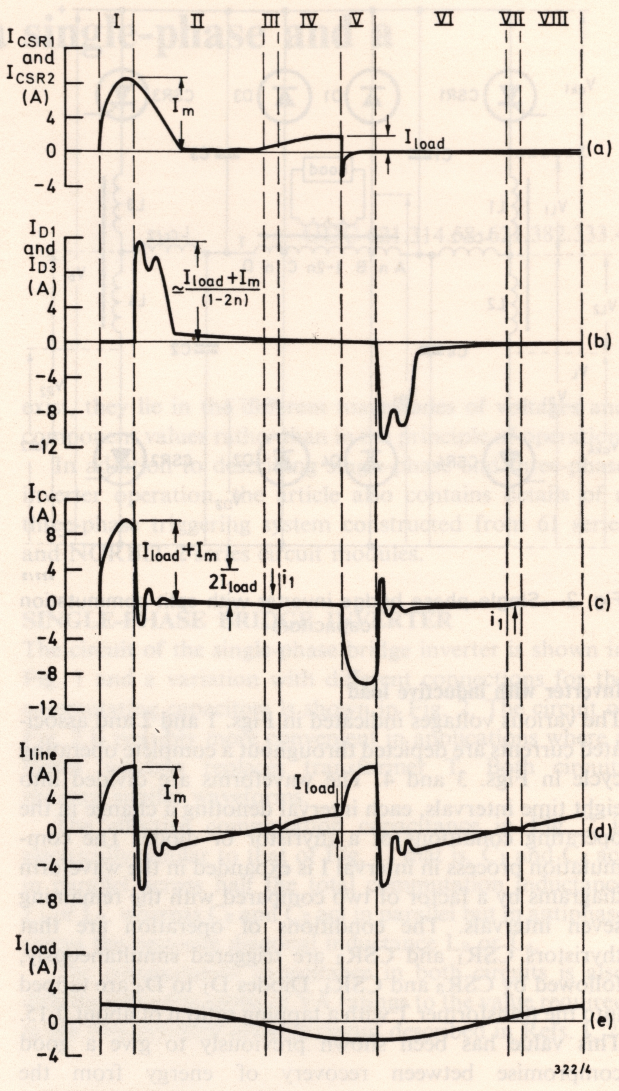


Fig. 4—Current waveforms for inductive load

Interval IV

Thyristors CSR_1 and CSR_2 are now in normal conduction and diodes D_1 and D_2 have ceased conduction. The forward blocking voltage across CSR_4 (and CSR_3) has reduced to V_b volts (Fig. 3i), this also being the final voltage on the commutation capacitor (Fig. 3e).

Intervals V to VIII

Thyristors CSR_3 and CSR_4 are triggered into conduction in interval V, throwing reverse blocking voltages across CSR_1 and CSR_2. The complete process in intervals I to IV is now repeated through intervals V to VIII, but in a reverse sense.

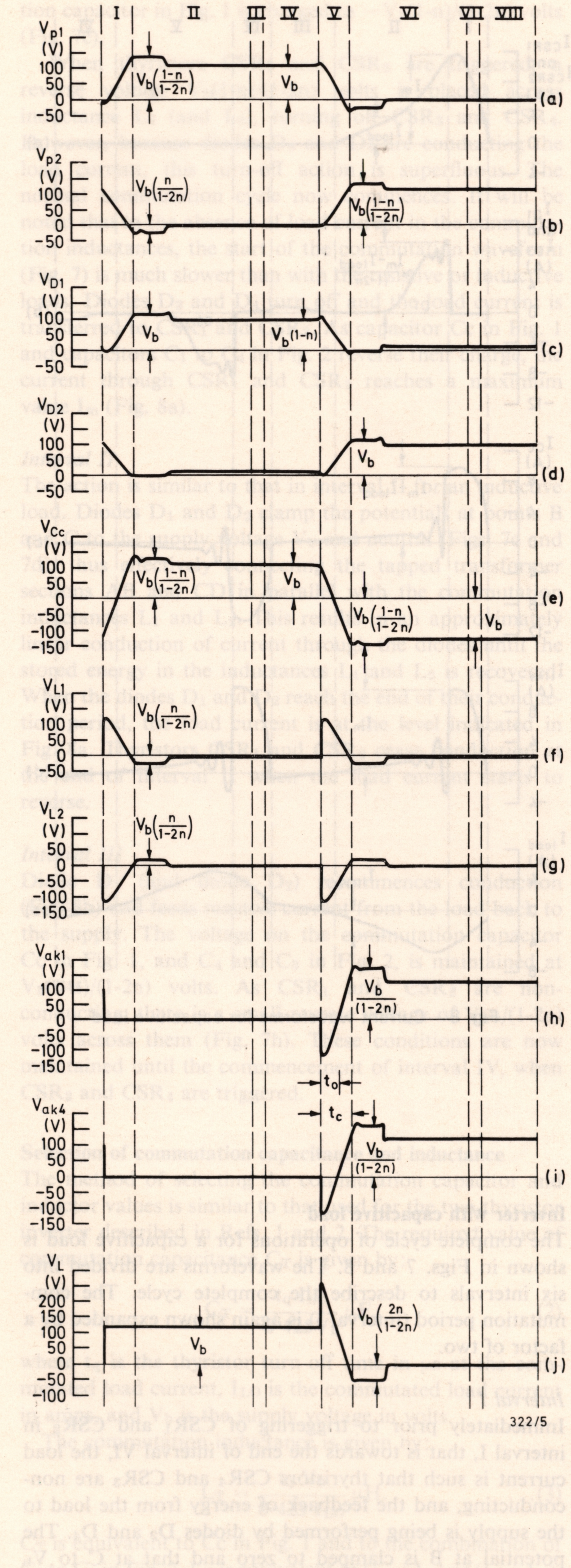


Fig. 5—Voltage waveforms for resistive load

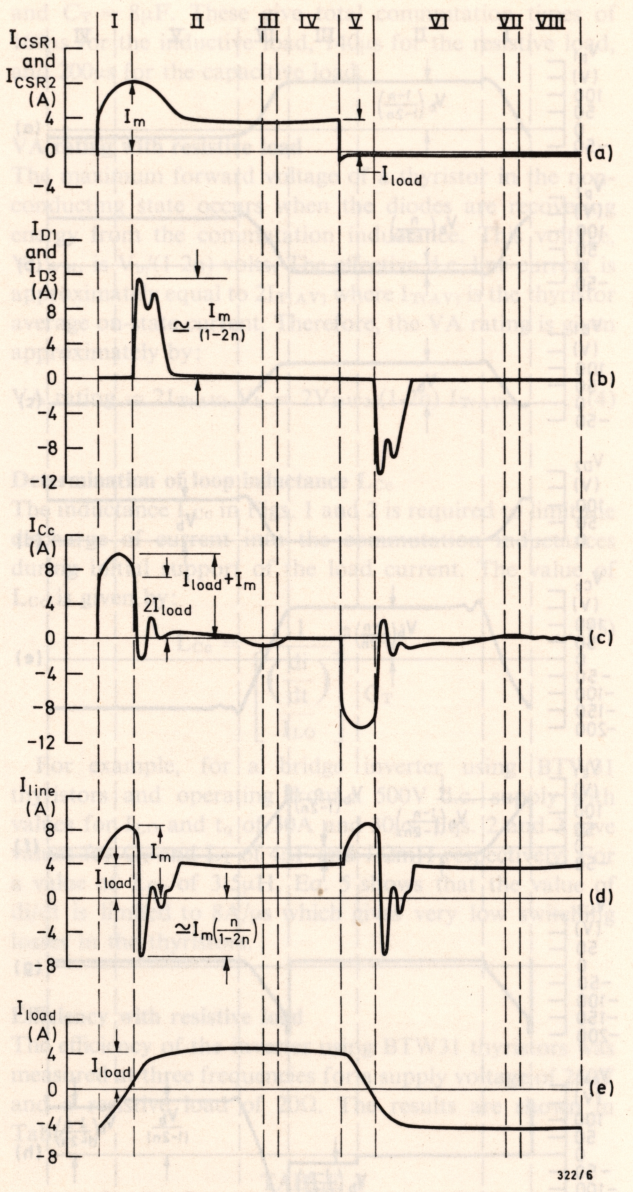


Fig. 6—Current waveforms for resistive load

Inverter with resistive load

The waveforms for the inverter operating into a resistive load are shown in Figs. 5 and 6, drawn to the same scale. The commutation cycle is similar to that for the inductive load. However, during the commutation period the load current is reversed. In consequence, thyristors CSR_1 and CSR_2 conduct continuously through intervals I, II, III, and IV (Fig. 6a), and diodes D_1 and D_2 cease conduction after returning energy from L_1 and L_4 to the supply line (Fig. 6b).

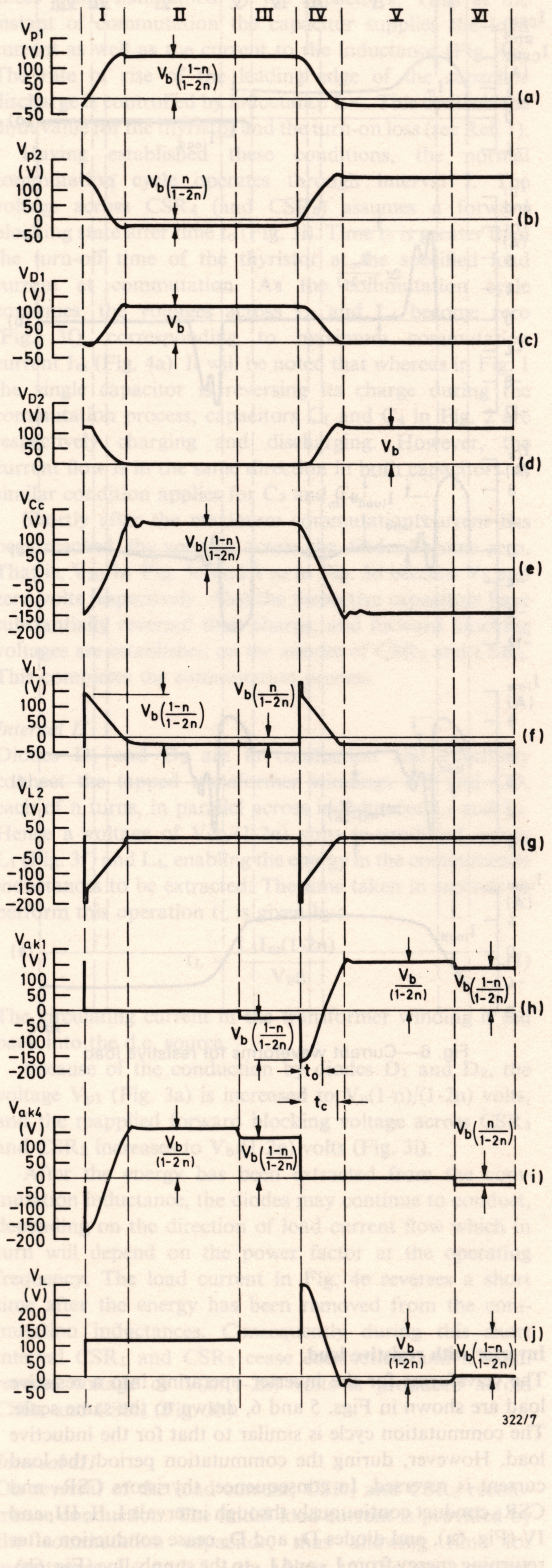


Fig. 7—Voltage waveforms for capacitive load

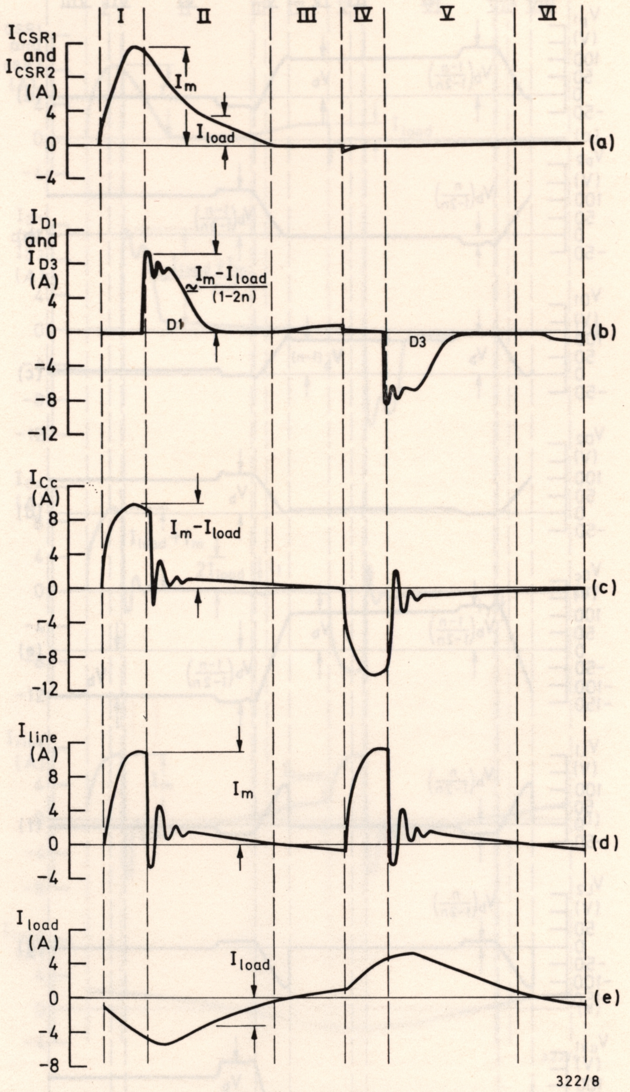


Fig. 8—Current waveforms for capacitive load

Inverter with capacitive load

The complete cycle of operations for a capacitive load is shown in Figs. 7 and 8. The waveforms are divided into six intervals to describe the complete cycle. The commutation period (interval I) is again shown expanded by a factor of two.

Interval I

Immediately prior to triggering of CSR_1 and CSR_2 in interval I, that is towards the end of interval VI, the load current is such that thyristors CSR_4 and CSR_3 are non-conducting, and the feedback of energy from the load to the supply is being performed by diodes D_3 and D_4. The potential at B is clamped to zero and that at C to V_b (Figs. 7c, d), resulting in a small reverse bias of $V_b n/(1\text{-}2n)$ volts across CSR_3 and CSR_4 (Fig. 7i). Also, the commutation capacitor in Fig. 1 is charged to $-V_b(1\text{-}n)/(1\text{-}2n)$ volts (Fig. 7e).

When thyristors CSR_1 and CSR_2 are triggered, a reverse voltage $V_b(1\text{-}n)/(1\text{-}2n)$ volts is placed across inductance L_2 (and L_3), turning off CSR_3 and CSR_4. However, because diodes D_3 and D_4 are conducting the load current, this turn-off action is superfluous. The normal commutation cycle now commences. It will be noted that in the absence of load current in the commutation inductances, the start of the commutation waveform (Fig. 7) is much slower than with the resistive or inductive loads. Diodes D_3 and D_4 turn off and the load current is transferred to CSR_1 and CSR_2. As capacitor C_c in Fig. 1 and capacitors C_1 to C_4 in Fig. 2 reverse their charge, the current through CSR_1 and CSR_2 reaches a maximum value I_m (Fig. 8a).

Interval II

The action is similar to that in interval II for an inductive load. Diodes D_1 and D_2 clamp the potentials at points B and C to the supply voltage V_b and neutral (Figs. 7c and 7d), thus effectively connecting the tapped transformer sections AB and CD in parallel with the commutation inductances L_1 and L_2. This results in an approximately linear conduction of current through the diodes until the stored energy in the inductances L_1 and L_2 is recovered. When the diodes D_1 and D_2 reach the end of their conduction period, the load current is at the level indicated in Fig. 8a. Thyristors CSR_1 and CSR_2 cease conduction at the end of interval II when the load current starts to reverse.

Interval III

Diode D_1 (and diode D_2) recommences conduction (Fig. 8b) and feeds reactive current from the load back to the supply. The voltage on the commutation capacitor C_c in Fig. 1, and C_4 and C_3 in Fig. 2, is maintained at $V_b(1\text{-}n)/(1\text{-}2n)$ volts. As CSR_1 and CSR_2 are non-conducting, there is a small reverse voltage of $V_b n/(1\text{-}2n)$ volts across them (Fig. 7h). These conditions are now maintained until the commencement of interval IV, when CSR_3 and CSR_4 are triggered.

Selection of commutation capacitance and inductance

The method of selecting the commutation capacitor and inductor values is similar to that used for the two-thyristor inverter described in Refs. 1 and 2. The required value of commutation capacitance C_T is given by:

$$C_T = \frac{t_q\, I_{LO}}{0{\cdot}425 V_b}\ \mu F, \qquad \ldots(2)$$

where t_q is the thyristor turn-off time in μs at the commutated load current, I_{LO} is the commutated load current in amps, and V_b is the supply voltage in volts.

The commutation inductance is given by:

$$L_T = \frac{t_q\, V_b}{0{\cdot}425\, I_{LO}}\ \mu H. \qquad \ldots(3)$$

C_T is equivalent to C_c in Fig. 1 and to the combination of C_1 to C_4 in Fig. 2. L_T is equivalent to (L_1+L_2) or (L_3+L_4). The values chosen for the test conditions were $L_T = 2\text{mH}$ and $C_T = 8\mu F$. These give total commutation times of 160μs for the inductive load, 140μs for the resistive load, and 200μs for the capacitive load.

VA rating with resistive load

The maximum forward voltage of a thyristor in the non-conducting state occurs when the diodes are recovering energy from the commutation inductance. This voltage, V_{DWM}, is $V_b/(1\text{-}2n)$ volts. The effective d.c. line current is approximately equal to $2I_{T(AV)}$ where $I_{T(AV)}$ is the thyristor average on-state current. Therefore, the VA rating is given approximately by:

$$\text{VA rating} = 2I_{T(AV)}\, V_b = 2V_{DWM}(1\text{-}2n)\, I_{T(AV)}. \qquad \ldots(4)$$

Determination of loop inductance L_{Cc}

The inductance L_{Cc} in Figs. 1 and 2 is required to limit the discharge of current into the commutation inductances during initial support of the load current. The value of L_{Cc} is given by:

$$L_{Cc} = \frac{1}{\left[\dfrac{\left(\frac{di}{dt}\right)}{I_{LO}}\right]^2 C_T} \qquad \ldots(5)$$

For example, for a bridge inverter using BTW31 thyristors and operating from a 500V d.c. supply with values for I_{LO} and t_q of 30A and 30μs, Eqs. 2 and 3 give values for C_T and L_T of 4μF and 1·2mH respectively. For a value of L_{Cc} of 3·5μH, Eq. 5 shows that the value of di/dt is limited to 8A/μs which gives very low switching losses in the thyristors.

Efficiency with resistive load

The efficiency of the inverter using BTW31 thyristors was measured at three frequencies for a supply voltage of 250V and a resistive load of 20Ω. The results are shown in Table 1.

TABLE 1

Efficiency of single-phase inverter with resistive load

Frequency (Hz)	Efficiency (%)
200	94
400	90
800	78

The measurements indicate a considerable fall-off in efficiency caused by commutation losses at frequencies above about 400Hz.

Trigger circuit for single-phase bridge inverter

The trigger circuit for the single-phase bridge inverter is shown in Fig. 9. It is similar to that described in Ref. 2. However, an additional TT61 trigger transformer is required because of the greater number of thyristors. A pulse blanking circuit is also added which is required for similar reasons to those given for the three-phase trigger system described later (page 216).

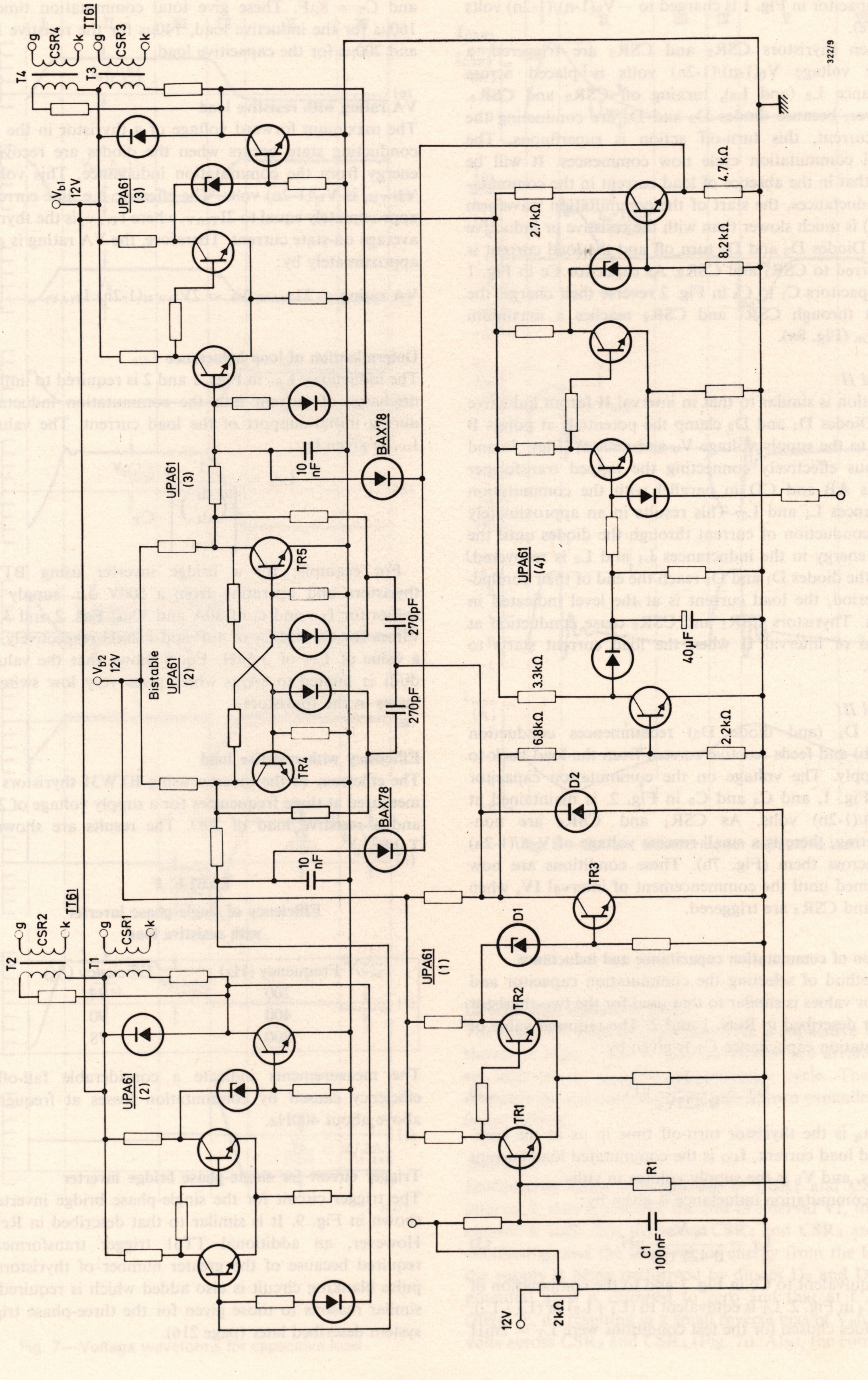

T4
CSR4
T3
CSR3
TT61
g
k
V_{b1} 12V
UPA61 (3)
BAX78
10 nF
UPA61 (3)
TR5
UPA61 (4)
270pF
Bistable UPA61 (2)
V_{b2} 12V
TR4
BAX78
10 nF
T2
CSR2
T1
CSR1
TT61
UPA61 (2)
UPA61 (1)
4.7kΩ
2.7kΩ
8.2kΩ
40µF
3.3kΩ
6.8kΩ
2.2kΩ
D2
TR3
D1
TR2
TR1
R1
C1 100nF
12V
2kΩ
322/9

Fig. 9—Trigger circuit for single-phase bridge inverter

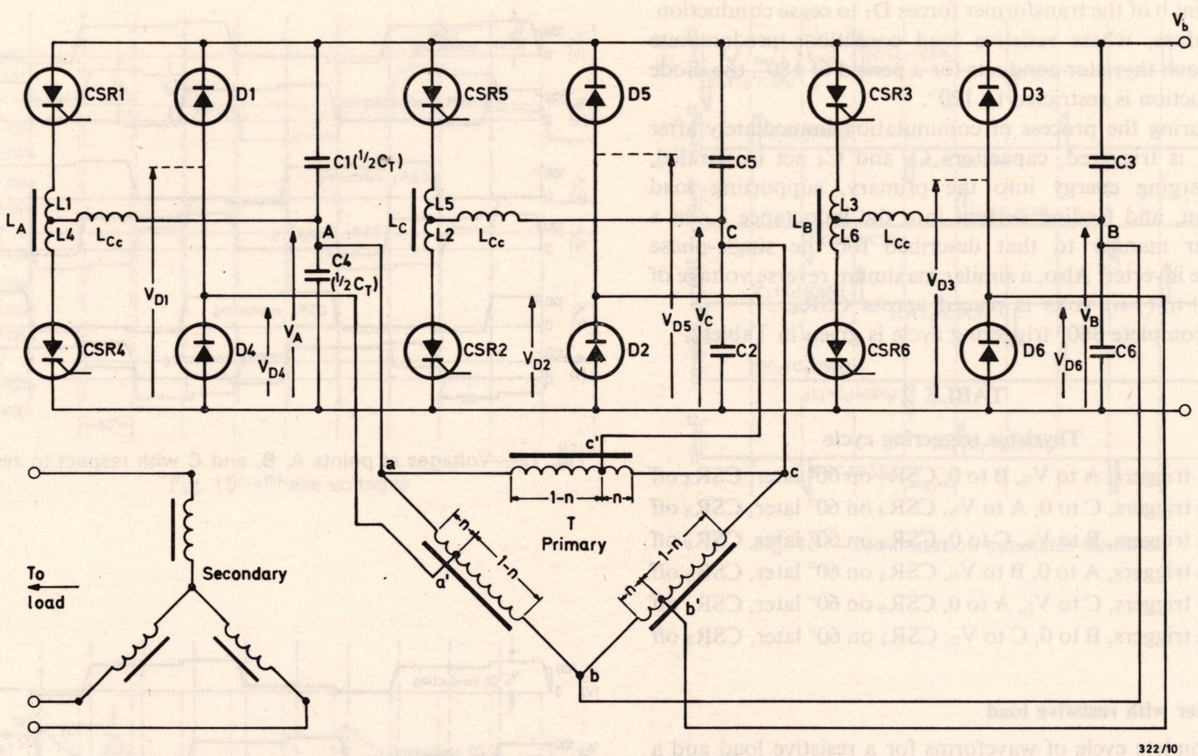

V_b
CSR1
D1
CSR5
D5
CSR3
D3
C1(½C_T)
C5
C3
L_A
L1
L4
L_{Cc}
A
C4 (½C_T)
V_{D1}
L_C
L5
L2
C
L_B
L3
L6
B
V_{D3}
V_A
V_{D4}
V_{D2}
V_{D5}
V_C
V_B
V_{D6}
CSR4
D4
CSR2
D2
C2
CSR6
D6
C6
a
c
c'
1-n
n
T
Primary
a'
b'
b
Secondary
To load
322/10

Fig. 10—Three-phase bridge inverter

THREE-PHASE BRIDGE INVERTER

The three-phase bridge inverter to be described follows logically from the single-phase bridge inverter, or more accurately from the single-phase half-bridge inverter. The circuit is shown in Fig. 10. Each section of the bridge, which incorporates a pair of thyristors, feeds into connection points a, b, and c of the three-phase delta-connected primary of transformer T. In each transformer winding, a tapping point is introduced which enables the diodes to return energy to the supply in a similar manner to that described for the single-phase system.

Thyristor trigger sequence

To produce the normal three-phase waveform pattern in terms of the 120° phase displacement between each phase, the conduction period of each thyristor must be 180°, and the triggering of each thyristor must take place at 60° intervals throughout a complete 360° cycle of operation.

In Fig. 10, the thyristors are numbered in sequence CSR_1 to CSR_6 corresponding to their triggering order in the 60° phase displacement pattern. The rotation of the phases within the transformer primary is in the sequence a, b, c. (This phase rotation corresponds to the three-phase sequence produced by the triggering circuits which are described later.) In addition, the diode taps in the primary of the transformer, shown as a′, b′, and c′, must be correctly positioned with respect to the triggering sequence of the thyristors to allow energy to be extracted from the commutation inductances immediately after the commutation period, and also to allow reactive energy in the load to be conducted back to the supply.

At any particular time, there are three thyristors conducting current. From Fig. 11, it will be seen that when thyristor CSR_1 starts to conduct, CSR_6 has a 120° current conduction period remaining and CSR_5 has a 60° conduction period remaining. For the triggering conditions shown in Fig. 11, with CSR_1 starting conduction and in turn commutating CSR_4, point A in Fig. 10 will rise to the potential of the supply V_b. A very short time after, if the potential at point b is zero, the potential at point a will cause diode D_1 to conduct. This condition will hold if CSR_6 is conducting. During the conduction period of D_1 the potential at A is raised to $V_b/(1\text{-}n)$ volts by auto-transformer action (see Fig. 12 later). After the remaining 120° conduction period of CSR_6 has been completed (Fig. 11), CSR_3 is triggered and the increase of potential

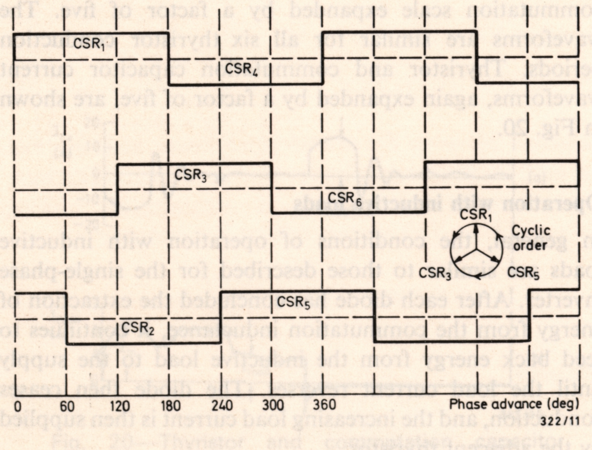

CSR_1
CSR_4
CSR_3
CSR_6
CSR_1
Cyclic order
CSR_3
CSR_5
CSR_5
CSR_2
0
60
120
180
240
300
360
Phase advance (deg)
322/11

Fig. 11—Anticlockwise triggering of thyristors

at point b of the transformer forces D_1 to cease conduction. Therefore, where resistive load conditions predominate and each thyristor conducts for a period of 180°, the diode conduction is restricted to 120°.

During the process of commutation immediately after CSR$_1$ is triggered, capacitors C_1 and C_4 act in parallel, discharging energy into the primary, supporting load current, and feeding current into the inductance L_1 in a similar manner to that described for the single-phase bridge inverter. Also, a similar maximum reverse voltage of $V_b(1+n)/(1-n)$ volts is placed across CSR$_4$.

A complete 360° triggering cycle is given in Table 2.

TABLE 2

Thyristor triggering cycle

CSR$_1$ triggers, A to V_b, B to 0, CSR$_2$ on 60° later, CSR$_4$ off
CSR$_2$ triggers, C to 0, A to V_b, CSR$_3$ on 60° later, CSR$_5$ off
CSR$_3$ triggers, B to V_b, C to 0, CSR$_4$ on 60° later, CSR$_6$ off
CSR$_4$ triggers, A to 0, B to V_b, CSR$_5$ on 60° later, CSR$_1$ off
CSR$_5$ triggers, C to V_b, A to 0, CSR$_6$ on 60° later, CSR$_2$ off
CSR$_6$ triggers, B to 0, C to V_b, CSR$_1$ on 60° later, CSR$_3$ off

Inverter with resistive load

A complete cycle of waveforms for a resistive load and a supply voltage of 120V is shown in Figs. 12 to 20. The waveforms have been idealized to explain the action more clearly. The actual waveforms contain a certain amount of ripple caused by commutation action.

Fig. 12 shows the voltages measured at points A, B, and C with respect to neutral. Fig. 13 shows the voltages associated with the diodes. It will be noted that when the lower thyristors and diodes in Fig. 10 are conducting, a reverse voltage $V_b n/(1-n)$ volts appears at points A, B, and C. The voltages across the thyristors are shown in Fig. 14.

The resultant phase voltages for the inverter, measured from A to C, B to A, and B to C, are shown in Fig. 15. It will be noted that a small offset voltage on each side of the zero line is produced immediately after commutation. This is due to diode conduction.

Figs. 16, 17 and 18 show diode current, thyristor current and commutation capacitor current in order of conduction for an operating frequency of about 300Hz. Typical voltage waveforms for the circuit are shown in Fig. 19 with the commutation scale expanded by a factor of five. The waveforms are similar for all six thyristor conduction periods. Thyristor and commutation capacitor current waveforms, again expanded by a factor of five, are shown in Fig. 20.

Operation with inductive loads

In general, the conditions of operation with inductive loads are similar to those described for the single-phase inverter. After each diode has concluded the extraction of energy from the commutation inductance, it continues to feed back energy from the inductive load to the supply until the load current reverses. The diode then ceases conduction, and the increasing load current is then supplied by the adjacent thyristor.

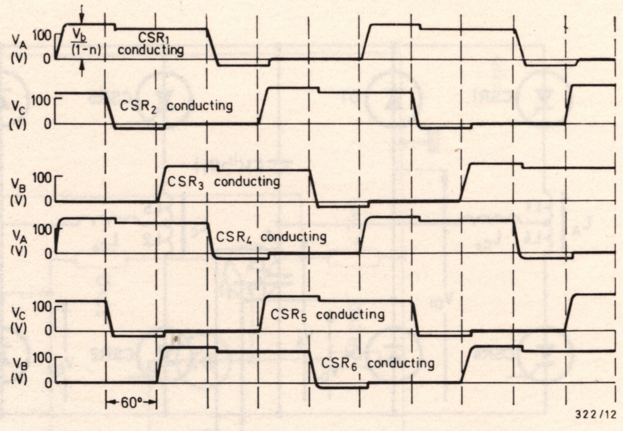


Fig. 12—Voltages at points A, B, and C with respect to zero

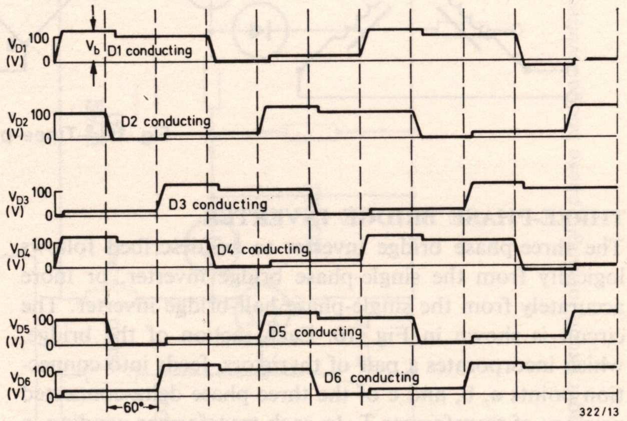


Fig. 13—Voltages associated with the diodes with respect to zero

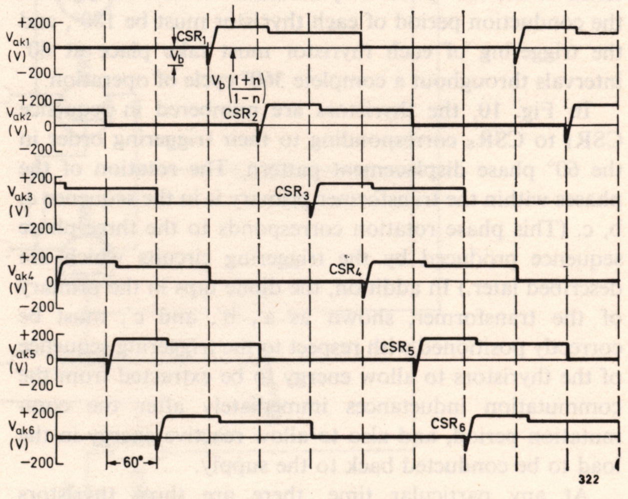


Fig. 14—Voltages across the thyristors

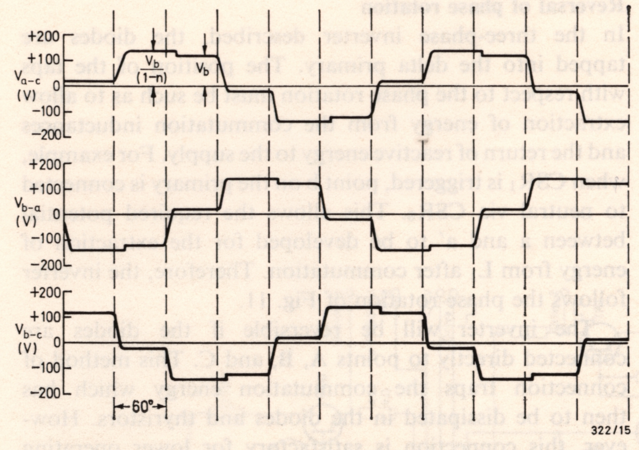


Fig. 15—Phase voltages

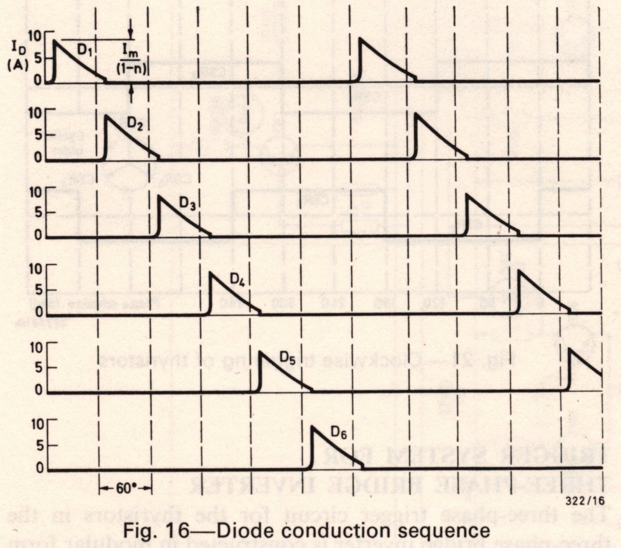


Fig. 16—Diode conduction sequence

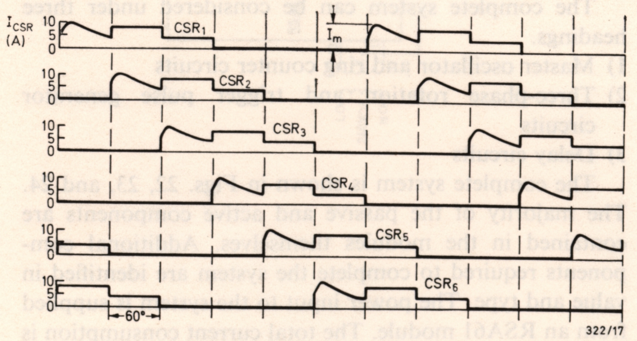


Fig. 17—Thyristor conduction sequence

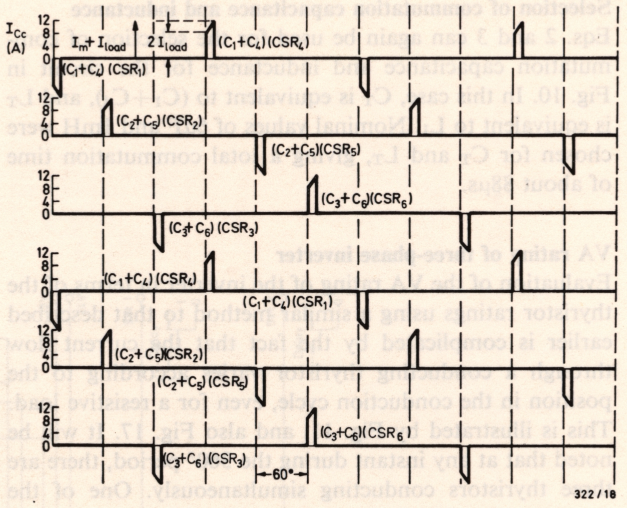


Fig. 18—Commutation capacitor currents

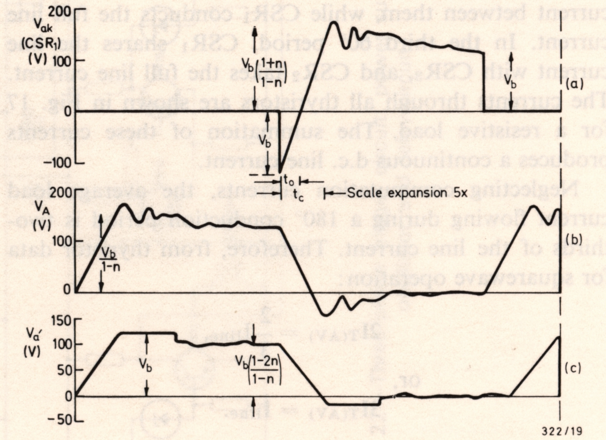


Fig. 19—Voltage waveforms

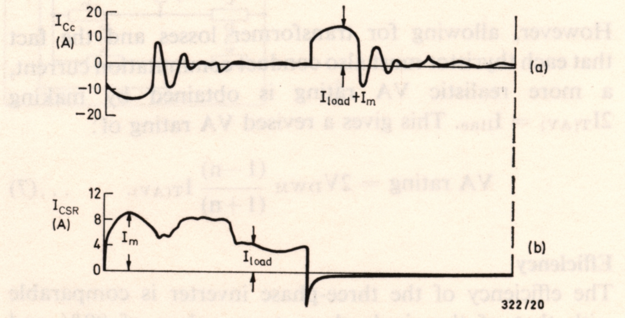


Fig. 20—Thyristor and commutation capacitor current waveforms

Selection of commutation capacitance and inductance

Eqs. 2 and 3 can again be used for the selection of commutation capacitance and inductance for the circuit in Fig. 10. In this case, C_T is equivalent to (C_1+C_4), and L_T is equivalent to L_1. Nominal values of 6μF and 1mH were chosen for C_T and L_T, giving a total commutation time of about 88μs.

VA rating of three-phase inverter

Evaluation of the VA rating of the inverter in terms of the thyristor ratings using a similar method to that described earlier is complicated by the fact that the current flow through a conducting thyristor varies according to the position in the conduction cycle, even for a resistive load. This is illustrated by Fig. 11, and also Fig. 17. It will be noted that at any instant during the 360° period, there are three thyristors conducting simultaneously. One of the three thyristors conducts the total line current while the other two share the line current between them.

When CSR_1 conducts as shown in Fig. 11, CSR_5 and CSR_6 are also in conduction. Over the first 60° period of conduction with CSR_1, this thyristor conducts half the line current in conjunction with CSR_5, whereas CSR_6 conducts the full line current. In the second 60° period, thyristors CSR_2 and CSR_6 are conducting, sharing the line current between them, while CSR_1 conducts the full line current. In the third 60° period, CSR_1 shares the line current with CSR_3, and CSR_2 takes the full line current. The currents through all thyristors are shown in Fig. 17 for a resistive load. The summation of these currents produces a continuous d.c. line current.

Neglecting commutation currents, the average load current flowing during a 180° conduction period is two-thirds of the line current. Therefore, from thyristor data for squarewave operation:

$$2I_{T(AV)} = \frac{2}{3} I_{line},$$

or,

$$3I_{T(AV)} = I_{line}.$$

The maximum forward voltage applied to a thyristor in the blocking state is $V_b\,(1+n)/(1-n)$ volts. That is:

$$V_b = V_{DWM}\frac{(1-n)}{(1+n)}.$$

Thus, the VA rating is given by:

$$\text{VA rating} = 3I_{T(AV)}\,V_b = 3V_{DWM}\frac{(1-n)}{(1+n)}I_{T(AV)}. \quad \ldots(6)$$

However, allowing for transformer losses and the fact that each thyristor must also conduct commutation current, a more realistic VA rating is obtained by making $2I_{T(AV)} = I_{line}$. This gives a revised VA rating of:

$$\text{VA rating} = 2V_{DWM}\frac{(1-n)}{(1+n)}I_{T(AV)}. \quad \ldots(7)$$

Efficiency

The efficiency of the three-phase inverter is comparable with that of the single-phase type, values of 90% and 82% being measured at 400Hz and 600Hz respectively.

Reversal of phase rotation

In the three-phase inverter described, the diodes are tapped into the delta primary. The position of the taps with respect to the phase rotation must be such as to allow extraction of energy from the commutation inductances and the return of reactive energy to the supply. For example, when CSR_1 is triggered, point b on the primary is connected to neutral via CSR_6. This allows the required potential between a and a′ to be developed for the extraction of energy from L_1 after commutation. Therefore, the inverter follows the phase rotation of Fig. 11.

The inverter will be reversible if the diodes are connected directly to points A, B, and C. This method of connection traps the commutation energy which has then to be dissipated in the diodes and thyristors. However, this connection is satisfactory for lower operating frequencies. Fig. 21 shows the reversed order (clockwise) of thyristor triggering.

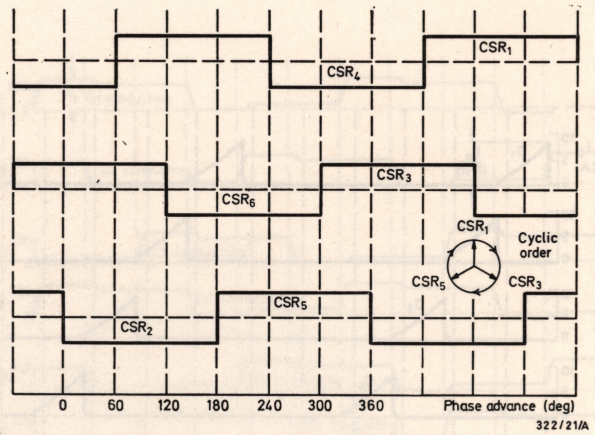


Fig. 21—Clockwise triggering of thyristors

TRIGGER SYSTEM FOR THREE-PHASE BRIDGE INVERTER

The three-phase trigger circuit for the thyristors in the three-phase bridge inverter is constructed in modular form using a combination of 61 series modules (Ref. 3), and FF90 modules from the NORBIT 2 range. The circuit is required to provide a set of trigger pulses in three-phase sequence whose direction of phase rotation can be reversed by applying a negative bias to the appropriate 2NOR61 modules contained in the circuit.

The complete system can be considered under three headings.

1) Master oscillator and ring counter circuits
2) Three-phase rotation and trigger pulse generator circuits
3) Delay circuits

The complete system is shown in Figs. 22, 23, and 24. The majority of the passive and active components are contained in the modules themselves. Additional components required to complete the system are identified in value and type. The power input to the system is supplied from an RSA61 module. The total current consumption is approximately 260mA from a 24V supply.

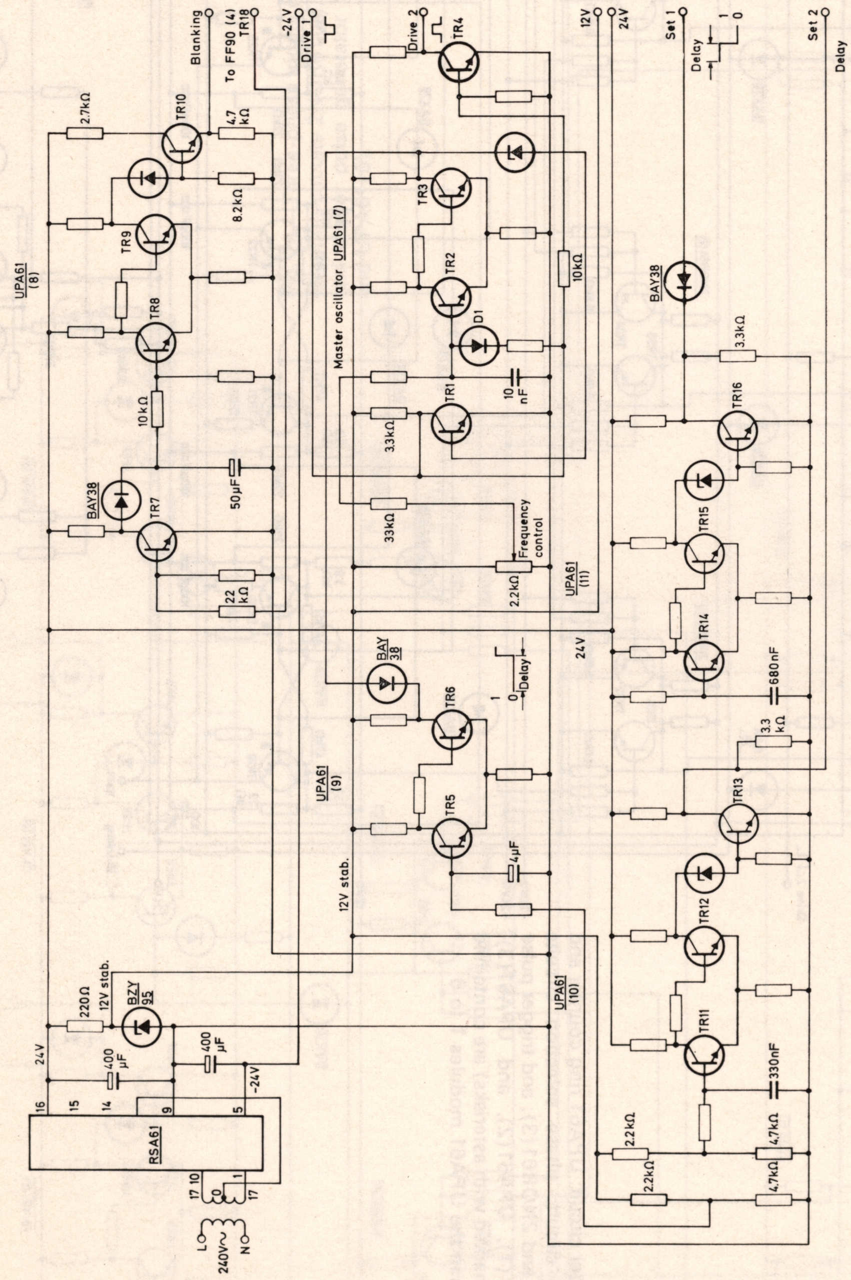


Fig. 22—Three-phase trigger circuit: power supply, master oscillator, and delay circuit

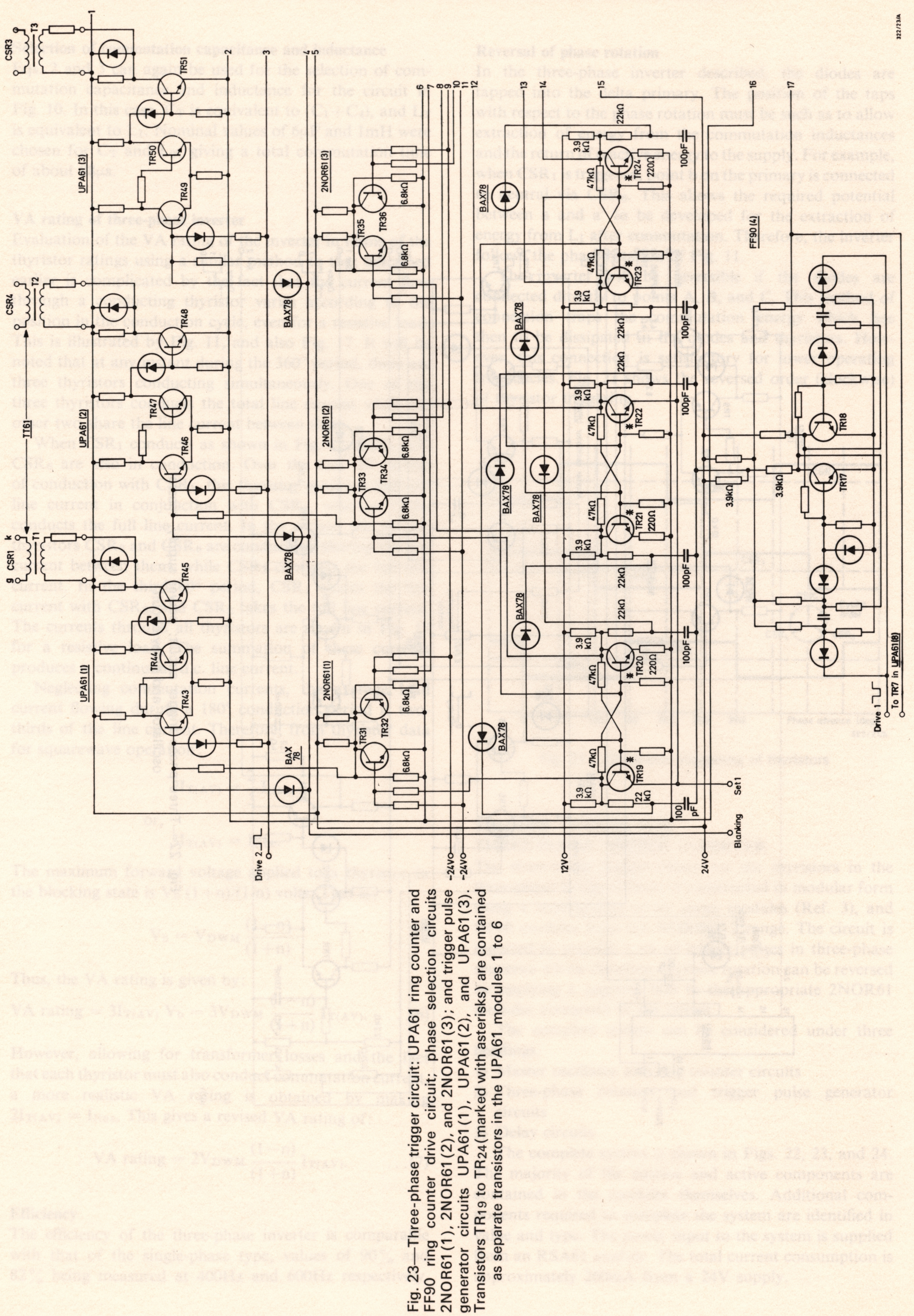

CSR1
CSR3
CSR4
T1
T2
T3
TT61
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
TR31
TR32
TR33
TR34
TR35
TR36
TR43
TR44
TR45
TR46
TR47
TR48
TR49
TR50
TR51
UPA61(1)
UPA61(2)
UPA61(3)
2NOR61(1)
2NOR61(2)
2NOR61(3)
FF90(4)
BAX78
3.9kΩ
47kΩ
22kΩ
220Ω
100pF
6.8kΩ
Drive 1
Drive 2
Set 1
Blanking
12V0
24V0
−2V0
To TR7 in UPA61(8)
3227/23A

Fig. 23—Three-phase trigger circuit: UPA61 ring counter and FF90 ring counter drive circuit; phase selection circuits 2NOR61(1), 2NOR61(2), and 2NOR61(3); and trigger pulse generator circuits UPA61(1), UPA61(2), and UPA61(3). Transistors TR_{19} to TR_{24}(marked with asterisks) are contained as separate transistors in the UPA61 modules 1 to 6

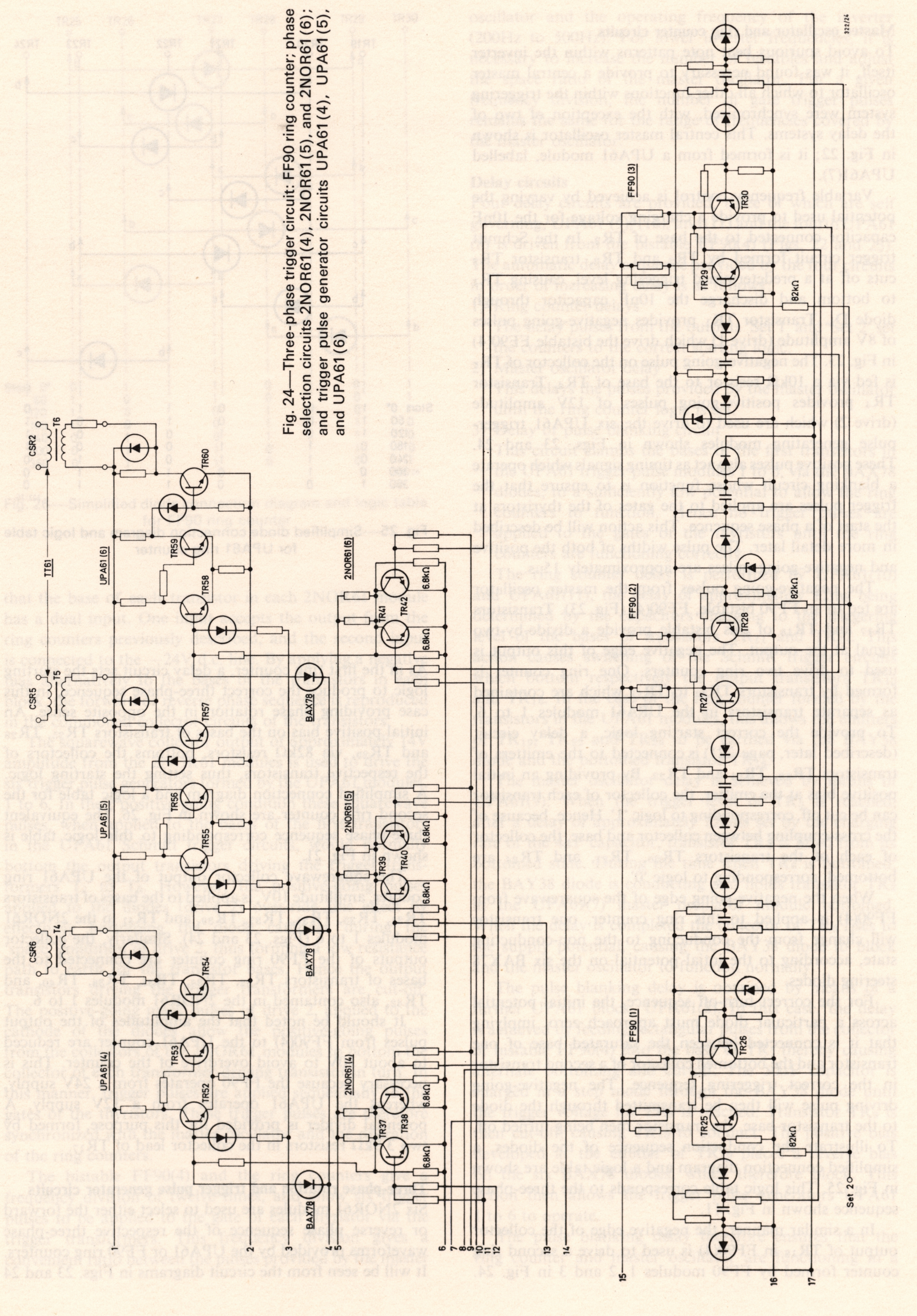

CSR2
CSR5
CSR6
T4
T5
T6
TT61
TR25
TR26
TR27
TR28
TR29
TR30
TR37
TR38
TR39
TR40
TR41
TR42
TR52
TR53
TR54
TR55
TR56
TR57
TR58
TR59
TR60
UPA61(4)
UPA61(5)
UPA61(6)
2NOR61(4)
2NOR61(5)
2NOR61(6)
FF90(1)
FF90(2)
FF90(3)
BAX78
6.8kΩ
82kΩ
Set 2
3227/24

Fig. 24—Three-phase trigger circuit: FF90 ring counter; phase selection circuits 2NOR61(4), 2NOR61(5), and 2NOR61(6); and trigger pulse generator circuits UPA61(4), UPA61(5), and UPA61(6)

Master oscillator and ring counter circuits

To avoid spurious beat note patterns within the inverter itself, it was found necessary to provide a central master oscillator to which all other functions within the triggering system were synchronized, with the exception of two of the delay systems. This central master oscillator is shown in Fig. 22; it is formed from a UPA61 module, labelled UPA61(7).

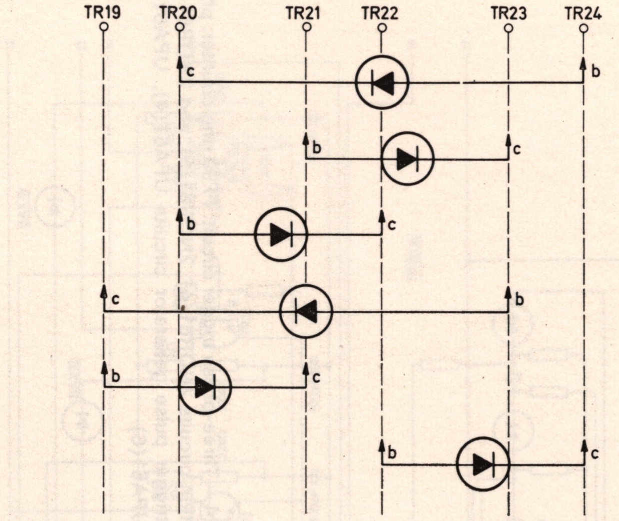
Variable frequency control is achieved by varying the potential used to provide a charging voltage for the 10nF capacitor connected to the base of TR$_2$. In the Schmitt trigger circuit formed by TR$_2$ and TR$_3$, transistor TR$_3$ cuts off at a predetermined triggering level, causing TR$_1$ to bottom and discharge the 10nF capacitor through diode D$_1$. Transistor TR$_1$ provides negative-going pulses of 8V amplitude (drive 1) which drive the bistable FF90(4) in Fig. 23. The negative-going pulse on the collector of TR$_1$ is fed via a 10kΩ resistor to the base of TR$_4$. Transistor TR$_4$ provides positive-going pulses of 12V amplitude (drive 2) which are used to drive the six UPA61 trigger-pulse generating modules shown in Figs. 23 and 24. These positive pulses also act as timing signals which operate a blanking circuit whose function is to ensure that the trigger pulses are applied to the gates of the thyristors at the start of a phase sequence. This action will be described in more detail later. The pulse widths of both the positive and negative-going pulses are approximately 15μs.

The negative-going pulses from the master oscillator are fed to an FF90 bistable, FF90(4) (Fig. 23). Transistors TR$_{17}$ and TR$_{18}$ of this bistable provide a divide-by-two signal at the output. The negative edge of this output is used to drive two ring counters. One ring counter is formed by transistors TR$_{22}$ to TR$_{23}$ which are contained as separate transistors in the UPA61 modules 1 to 6. To provide the correct starting logic, a delay circuit (described later, page 221) is connected to the emitters of transistors TR$_{19}$, TR$_{21}$ and TR$_{23}$. By providing an initial positive bias at the emitter, the collector of each transistor can be cut off, corresponding to logic '1'. Hence, because of the cross-coupling between collector and base, the collector of each of the transistors TR$_{20}$, TR$_{21}$, and TR$_{24}$ are bottomed, corresponding to logic '0'.

When the negative-going edge of the squarewave from FF90(4) is applied to this ring counter, one transistor will change from the conducting to the non-conducting state, according to the intial potential on the six BAX78 steering diodes.

For the correct turn-off sequence, the initial potential across a particular diode must approach zero, implying that it is connected between the saturated base of one transistor and the bottomed collector of a second transistor in the correct triggering sequence. The negative-going driving pulse will then be transmitted through the diode to the transistor base, the transistor then being turned off. To illustrate the conduction sequence of the diodes, a simplified connection diagram and a logic table are shown in Fig. 25. This logic table corresponds to the three-phase sequence shown in Fig. 11.

In a similar manner, the negative edge of the collector output of TR$_{18}$ in FF90(4) is used to drive a second ring counter formed by FF90 modules 1, 2 and 3 in Fig. 24.



	TR19	TR20	TR21	TR22	TR23	TR24
Start 0°	1	0	0	1	1	0
60	1	0	0	1	0	1
120	1	0	1	0	0	1
180	0	1	1	0	0	1
240	0	1	1	0	1	0
300	0	1	0	1	1	0
360	1	0	0	1	1	0

322/25

Fig. 25—Simplified diode connection diagram and logic table for UPA61 ring counter

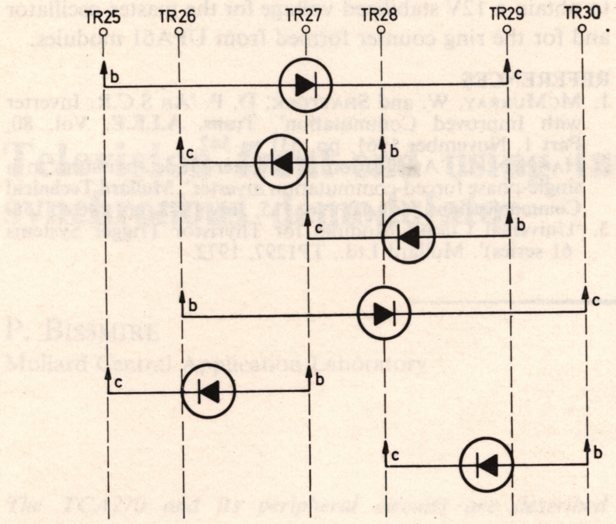
As in the first ring counter, a delay circuit sets the starting logic to produce the correct three-phase sequence, in this case providing phase rotation in the opposite sense. An initial positive bias on the bases of transistors TR$_{25}$, TR$_{28}$ and TR$_{29}$, via 82kΩ resistors, bottoms the collectors of the respective transistors, thus setting the starting logic. A simplified connection diagram and a logic table for the second ring counter are shown in Fig. 26. The equivalent three-phase sequence corresponding to this logic table is shown in Fig. 21.

The squarewave collector output of the UPA61 ring counter, amplitude 10V, is applied to the bases of transistors TR$_{31}$, TR$_{33}$, TR$_{35}$, TR$_{37}$, TR$_{39}$, and TR$_{41}$ in the 2NOR61 modules 1 to 6 (Figs. 23 and 24). Similarly, the collector outputs of the FF90 ring counter are connected to the bases of transistors TR$_{32}$, TR$_{34}$, TR$_{36}$, TR$_{38}$, TR$_{40}$, and TR$_{42}$, also contained in the 2NOR61 modules 1 to 6.

It should be noted that the amplitudes of the output pulses from FF90(4) to the UPA61 counter are reduced to about 10V to avoid overdrive of the counter. This is necessary because the FF90 operates from a 24V supply, whereas the UPA61 operates from a 12V supply. A potential divider is provided for this purpose, formed by two 3·9kΩ resistors in the collector lead of TR$_{17}$.

Three-phase rotation and trigger pulse generator circuits

Six 2NOR61 modules are used to select either the forward or reverse phase sequence of the respective three-phase waveforms provided by the UPA61 or FF90 ring counters. It will be seen from the circuit diagrams in Figs. 23 and 24 that the base of each transistor in each 2NOR61 module has a dual input. One input accepts the output from the ring counters previously described, and the second input is connected to the −24V d.c. line. By applying a negative bias alternatively to the bases of the transistors in each block, the forward or reverse phase sequence is reproduced in the commoned collector circuits of the transistors.



	TR25	TR26	TR27	TR28	TR29	TR30
Start 0°	0	1	1	0	0	1
60	1	0	1	0	0	1
120	1	0	0	1	0	1
180	1	0	0	1	1	0
240	0	1	0	1	1	0
300	0	1	1	0	1	0
360	0	1	1	0	0	1

322/26

Fig. 26—Simplified diode connection diagram and logic table for FF90 ring counter

The squarewave collector output of approximately 14V amplitude from the 2NOR61 modules is used to drive the six trigger pulse generators formed by the UPA61 modules, 1 to 6. In their positive-going condition these squarewave pulses, when applied to the bases of the first transistors in the UPA61 Schmitt trigger circuits, would normally bottom the output transistors driving the trigger transformers T$_1$ to T$_6$. However, the positive-going pulses applied to the diodes (drive 2) over-ride this effect by effectively bottoming the diode cathodes during the 'space' condition of drive 2, thus forming a low resistance path to earth for the transistor bases. Hence the output transistors driving the trigger transformers are cut-off. The positive-going mark pulses of drive 2, applied to the cathode of the diodes allow the positive-going pulses from the collectors of the 2NOR61 modules to bottom the collector of each transformer-driving transistor in turn. In this manner, trigger pulses are applied sequentially to the gates of the thyristors. These trigger pulses are therefore synchronized with the master oscillator and the operation of the ring counters.

The bistable FF90(4) and the ring counters give a frequency division of twelve times, and allow six trigger pulses to be applied to the gate of each thyristor via the trigger transformers. This frequency division gives a convenient ratio between the pulses provided by the master oscillator and the operating frequency of the inverter (200Hz to 500Hz). For lower inverter frequencies, it is necessary to increase the number of bistables and adjust the space ratio of the master oscillator. For a given frequency division, the number of gate trigger pulses remains the same for the range of frequencies covered by the master oscillator.

Delay circuits

Four delay circuits are provided, three of which are self governing, UPA61 (9), (10), and (11) and the fourth UPA61 (8) is driven from the bistable FF90(4) (Figs. 22 and 23). The automatic delay sequence provided by the four circuits in order of increasing delay is as follows:

1) Ring counter delays
   The delay pulses from the outputs 'Set 1' and 'Set 2' set the counters to the correct starting logic.
2) Master oscillator delay
   This delays the pulses provided by the master oscillator until the ring counter logic is set.
3) Delay or pulse blanking circuit
   This circuit clamps the bases of the first transistors in the UPA61 trigger pulse modules 1 to 6, via the BAX78 diodes, to a sufficiently low potential to allow the ring counters to function. Hence no trigger pulses are applied to the gates of the thyristors until the ring counters are functioning correctly.

The ring counter delay is performed by UPA61(10) and UPA61(11), the delay of approximately 12ms being determined by the capacitors charging to the triggering level of the bases of transistors TR$_{11}$ and TR$_{14}$. This action causes switching of the Schmitt trigger circuits which bottom respectively the output transistors TR$_{13}$ and TR$_{16}$. In the case of the ring counter formed by the transistors in the UPA61 modules, this allows the emitters of TR$_{19}$, TR$_{22}$ and TR$_{23}$ to be earthed via the BAY38 diode and the bottomed transistor TR$_{16}$.

The master oscillator delay is achieved by means of UPA61(9). When the trigger level of TR$_5$ is reached, after a delay of approximately 120ms set by the charging rate of the 4μF capacitor, transistor TR$_6$ is lifted from its bottomed state. During the time when TR$_6$ is bottomed, the BAY38 diode is conducting and holds transistor TR$_2$ in the UPA61(7) master oscillator module bottomed. When the delay is completed the collector of TR$_6$ rises to the supply potential, causing the BAY38 diode to block and the master oscillator to function normally.

The pulse blanking delay is obtained by means of a further UPA61 block, UPA61(8). In this case, the delay is achieved by feeding rectangular pulses from the collector of bistable FF90(4) into the base of TR$_7$ thereby causing alternate bottoming and cut-off. The 50μF capacitor is charged in a step mode through the BAY38 diode until the trigger voltage for TR$_8$ is reached. Transistor TR$_9$ is then cut-off, causing TR$_{10}$ to conduct. The positive bias developed at the emitter of TR$_{10}$ places a reverse bias on the six BAX78 diodes, which therefore block. This action then allows the trigger pulse generators UPA61 1 to 6 to operate.

The pulse blanking delay therefore ensures that the ring counter and master oscillator are functioning in a normal synchronized mode before trigger pulses are applied to the thyristor gates. It also provides for switch-on of trigger pulses at the correct time.

Power supplies

The d.c. power supplies for the complete trigger circuit are provided by an RSA61 circuit module (Fig. 22). This provides both the +24V and −24V supplies.

An external voltage regulator diode, BZY95, is used to obtain a 12V stabilized voltage for the master oscillator and for the ring counter formed from UPA61 modules.

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1. McMurray, W. and Shattuck, D. P. 'An S.C.R. Inverter with Improved Commutation'. **Trans. A.I.E.E.** Vol. 80, Part 1, November 1961, pp. 531 to 542.
2. Hampson, L. 'Application of inverter-grade thyristors in a single-phase forced-commutation inverter', **Mullard Technical Communications,** Vol. 12, No. 115, July 1972, pp. 146 to 158.
3. 'Universal Circuit Modules for Thyristor Trigger Systems 61 series)'. Mullard Ltd., TP1297, 1972.

Television front-end using integrated circuit TCA270 synchronous demodulator

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Mullard Central Application Laboratory

UDC 621.397[621.376](TCA270)

The TCA270 and its peripheral circuits are described together with a complete television receiver front-end. This includes an ELC1043/06 tuner, a linear-phase filter, and a three-stage amplifier. The sensitivity is approximately 12μV e.m.f. into 75Ω, signal-to-noise ratio 40dB and overall video bandwidth up to 5·25MHz.

INTRODUCTION

A high quality receiver front-end (tuner, i.f. amplifier, vision and sound demodulators) has been designed and constructed using the TCA270, with a simple i.f. amplifier and a phase-linear i.f. filter. The front-end is equally suitable for monchrome and colour receivers. The complete front-end circuit and description are given later in this article.

The TCA270 is an integrated synchronous demodulator with reference generation by filtering and limiting the input signal. It is primarily intended for the demodulation of negatively modulated television signals. In addition to the demodulator, the device includes a video amplifier with interference noise suppression, a peak level (sync tip) a.g.c. detector with drivers for n.p.n. tuner and i.f. control stages, and an a.f.c. discriminator. Two video outputs of opposite polarity are provided. The internal circuit of the TCA270 is shown in Fig. 1. The application diagram of the TCA270 is shown in Fig. 2, and this circuit is used as the basis for the following description of the TCA270.

DEMODULATOR INPUT AND TANK CIRCUIT

A balanced input is provided at pins 1 and 2. The d.c. level is set internally, and the signal should be applied from a floating transformer winding or through coupling capacitors. An unbalanced signal may be applied to either pin, the other being decoupled. A fairly low source impedance should be maintained at frequencies above the operating frequency to avoid parasitic oscillations. The nominal input sensitivity is 70mV rms at envelope peaks.

A shunt-tuned tank circuit is connected across pins 14 and 15 to provide the reference carrier filtering. The coil should be wound so as to give a reasonably high Q_0 to minimise its contribution to the total damping; coil damping impairs the limiting action and thus the differential gain at low input levels.

The TCA270 presents a damping impedance of 6kΩ, giving an overall Q factor of about 50 with the 56pF tuning capacitance as shown in Fig. 2. This is the highest recommended Q factor, which gives good intermodulation but rather critical tuning, requiring the use of the a.f.c. facility. For cases where a.f.c. is not used a lower value of tuning capacitance should be used: 39pF gives a Q of 40, and 27pF a Q of 30.

VIDEO OUTPUTS

Two low impedance video outputs are provided, one positive-going and the other negative-going, both with a d.c. level of 6V and a peak amplitude of 3V. This is indicated diagrammatically in Fig. 3.

Noise protection

White noise inversion

Since interference noise is not phase correlated to the carrier it can result in an output of either polarity from a synchronous demodulator. Positive-going impulse noise can give rise to 'whiter than white' pulses which, on a colour tube or monochrome tube with low e.h.t., can result in large defocused blobs. A circuit is therefore incorporated in the TCA270 to detect signal excursions more than 0·6V above the effective zero carrier level and return them towards black in the output. This margin is chosen to allow for a reasonable degree of receiver detuning without inversion of sound and chrominance components in areas of high brightness and saturation. Noise inversion occurs in both video outputs of the device.

Sync inversion

A similar inversion system operates on pulses beyond the synchronising level. In this case excursions of pin 9 output of more than 0·35V beyond the synchronising level (measured dynamically), are returned to a level in the grey-to-black region. This inversion occurs in both outputs but the inversion at pin 10 occurs more promptly than that at pin 9. As pin 10 would be most often used to feed a sync-separator this is considered beneficial.

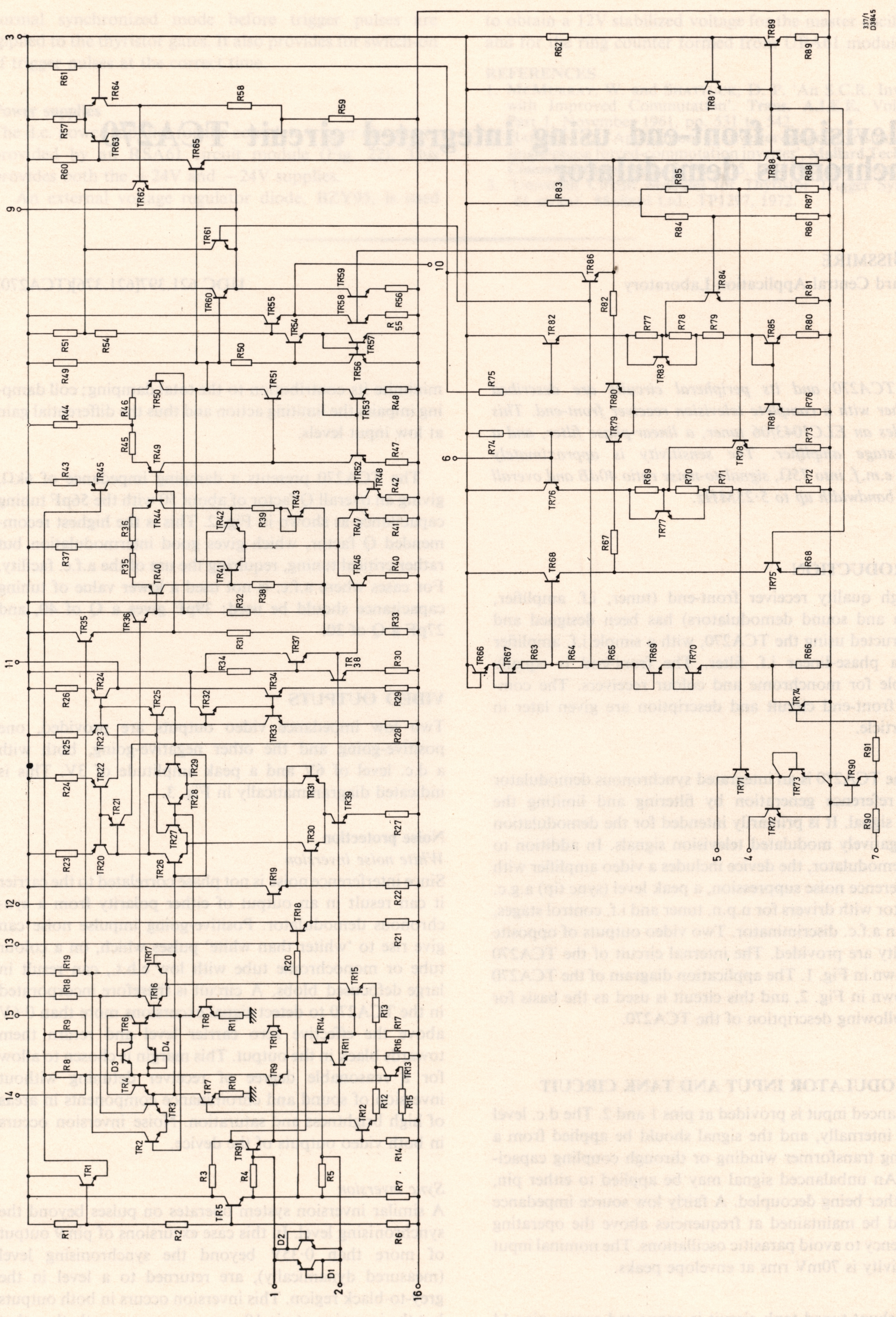

Fig. 1—TCA270 internal circuit

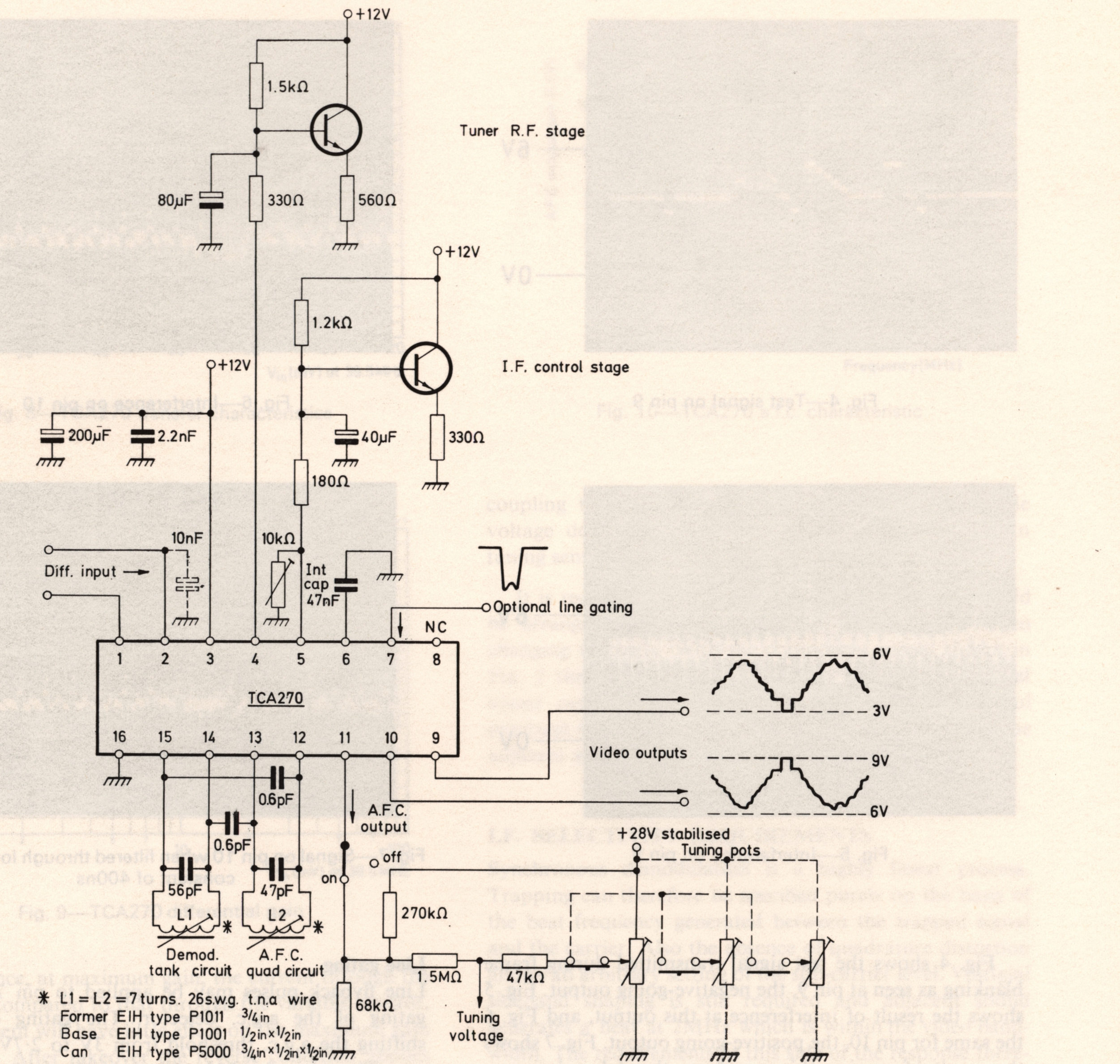
+12V
1.5kΩ
Tuner R.F. stage
80μF
330Ω
560Ω
+12V
1.2kΩ
I.F. control stage
+12V
200μF
2.2nF
40μF
330Ω
180Ω
Diff. input
10nF
10kΩ
Int cap 47nF
Optional line gating
NC
1 2 3 4 5 6 7 8
TCA270
16 15 14 13 12 11 10 9
6V
3V
Video outputs
9V
6V
0.6pF
0.6pF
A.F.C. output
+28V stabilised
Tuning pots
off
on
56pF
47pF
270kΩ
L1
L2
Demod. tank circuit
A.F.C. quad circuit
1.5MΩ
47kΩ
68kΩ
Tuning voltage
✱ L1 = L2 = 7 turns. 26s.w.g. t.n.a wire
Former EIH type P1011 3/4in
Base EIH type P1001 1/2in×1/2in
Can EIH type P5000 3/4in×1/2in×1/2in
Neosid core 4×0.5×6/900
337/2

Fig. 2—Application diagram of TCA270

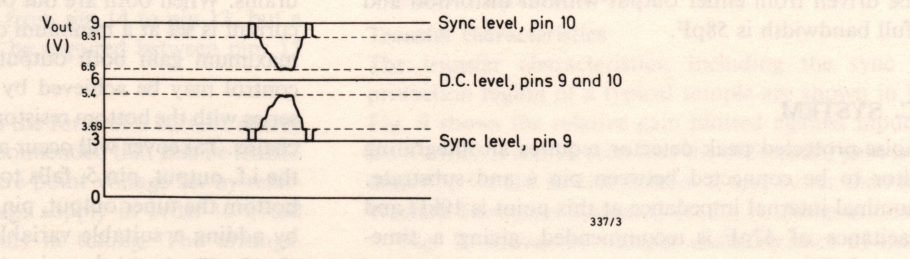

Fig. 3—Output signal levels

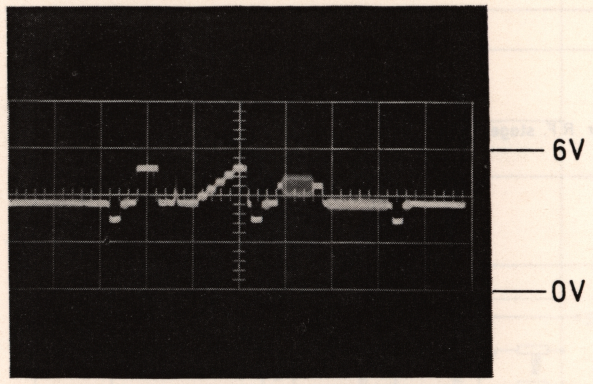

Fig. 4—Test signal on pin 9

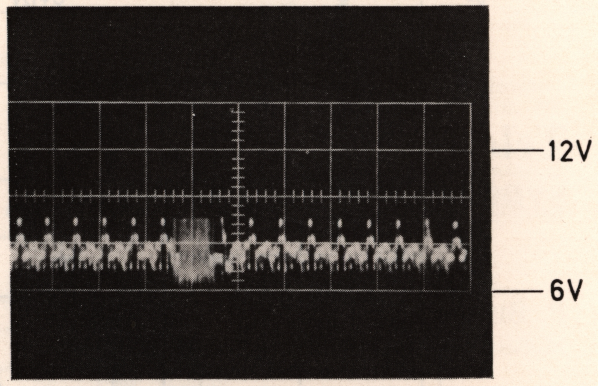

Fig. 6—Interference on pin 10

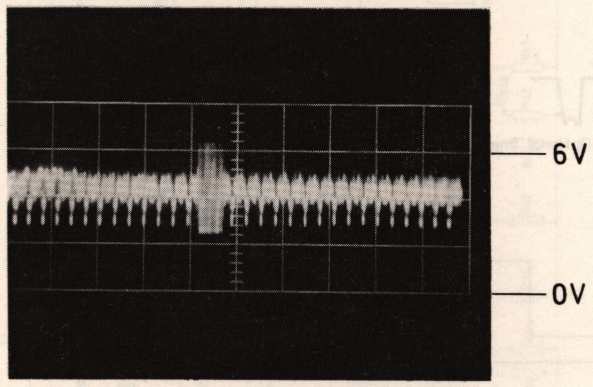

Fig. 5—Interference on pin 9

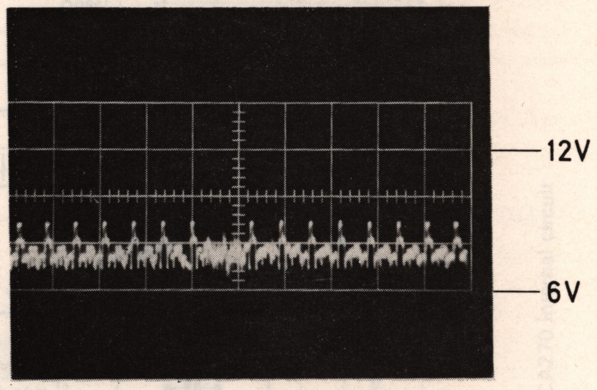

Fig. 7—Signal on pin 10 when filtered through low-pass time-constant of 400ns

Fig. 4 shows the test signal transmitted during frame blanking as seen at pin 9, the negative-going output. Fig. 5 shows the result of interference at this output, and Fig. 6 the same for pin 10, the positive-going output. Fig. 7 shows the result of passing this waveform through a low-pass time-constant of 400ns, from which it can be seen that, from the point of view of synchronisation, the effect is the same as would be achieved using a noise-gated sync-separator, that is, the loss of a sync pulse.

Output loading

No external load is required on either output, both being well suited to a.c. coupling. If d.c. coupling is used, positive conventional current flowing into the device should be much less than 1mA, as this current impairs its ability to drive a capacitive load. The maximum capacitance that may be driven from either output without distortion and with full bandwidth is 58pF.

A.G.C. SYSTEM

The noise-protected peak detector requires an integrating capacitor to be connected between pin 6 and substrate. The nominal internal impedance at this point is $10k\Omega$ and a capacitance of 47nF is recommended, giving a time-constant of $470\mu s$.

Line gating

Line flyback pulses may be applied to pin 7 to provide gating of the a.g.c. detector. The gating operates by shifting the a.g.c. threshold from 3V to 2·7V during line scan. The pulses should be negative-going with an amplitude of 3 to 14V (p.d. at the pin), provided that pin 7 does not go more positive than pin 3 (12V supply). The pulses may be a.c. or d.c. coupled.

For a.c. coupling a suitable capacitance is 22nF; for d.c. coupling the voltage at the pin during scan should exceed +1·5V and during flyback should be less than +0·5V.

Control outputs

The a.g.c. control outputs take the form of variable current drains. When both are out of bottoming the tuner control current is set at a minimum of six times that for the i.f. At maximum gain both outputs are turned on hard. Thus control may be achieved by inserting the two outputs in series with the bottom resistors of the appropriate base bias chains. Takeover will occur at a point where the current in the i.f. output, pin 5, falls to one sixth of that required to bottom the tuner output, pin 4. This point can be adjusted by adding a suitable variable resistor from pin 5 to substrate, so as to set the gain at which the above condition is

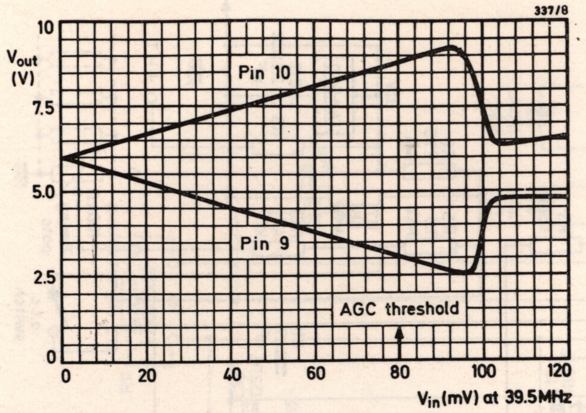

Fig. 8—TCA270 transfer characteristics

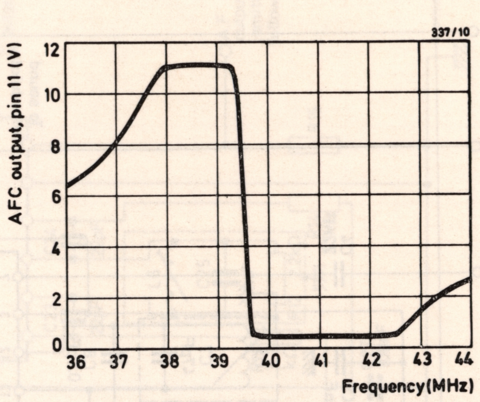

Fig. 10—TCA270 a.f.c. characteristic

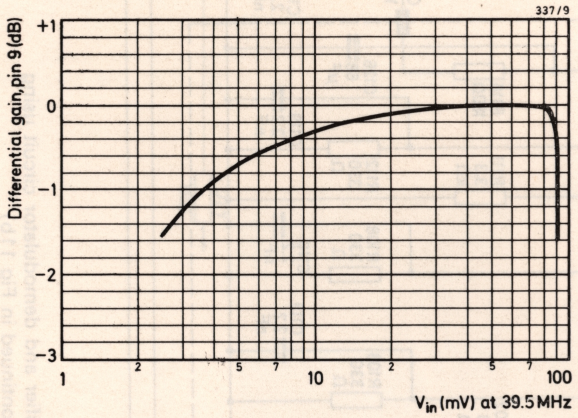

Fig. 9—TCA270 differential gain

satisfied. Since, at maximum gain, the current through the IC is large compared to that through the variable resistor, this adjustment will have little effect on the maximum gain bias setting. After takeover the reverse condition applies and little further control takes place in the i.f. stage.

The bottoming voltages at the control outputs are as follows:

i.f. ouput (pin 5)	+0·7 to +1·2V
tuner output (pin 4)	<+0·3V

A.F.C. SYSTEM

The a.f.c. discriminator requires a quadrature tank circuit to be connected to pins 12 and 13, with small capacitors coupling to pins 14 and 15, as shown in Fig. 2. In some cases the self-capacitance of a printed-wiring layout will be sufficient for the capacitance from pin 14 to pin 13, but a separate component will still be required between pins 15 and 12.

The output at pin 11 takes the form of a current source swinging about zero. It is recommended that this be loaded by about $50k\Omega$, with the centre-point voltage set by reference to the 28V tuning voltage supply in order to avoid introducing additional spreads in tuning. The arrangement shown has the added advantage that the network coupling the IC to the tuning voltage line may be made voltage dependent, to compensate for the variation in tuning sensitivity of the tuner over the band.

It is recommended that the a.f.c. switch shown should be arranged to disable the system automatically when changing channels. With the component values shown in Fig. 2 the receiver will not lock to the wanted channel sound carrier, but it is impossible to design a useful practical frequency lock system that will not lock to the adjacent sound carrier.

I.F. SELECTIVITY REQUIREMENTS

Synchronous demodulation is a highly linear process. Trapping can therefore be specified purely on the basis of the beat frequency generated between the trapped signal and the carrier. Also the absence of quadrature distortion allows an arbitrary setting of the sub-carrier level. Vestigial sideband shaping is still required and adjacent sound generates a beat at 2MHz which is within the video bandwidth. The requirements at this side of the response therefore remain unchanged. The products of own sound and adjacent vision are at 6MHz and 8MHz respectively and require less trapping, being outside the video bandwidth. However it is necessary to avoid either of these signals reaching the sync noise-protection threshold, especially where the sync pulses have overshot. The recommended trapping levels are therefore:

$$\left.\begin{array}{ll}\text{own sound} & >20\text{dB}\\ \text{adjacent vision} & >27\text{dB}\end{array}\right\}\text{ relative to carrier}$$

TCA270 PERFORMANCE

Transfer characteristics

The transfer characteristics, including the sync noise-protection region of a typical sample are shown in Fig. 8. Fig. 9 shows the relative gain plotted against input level, from which it can be seen that the differential gain is better than 4% for the British System I, and better than 8% for Western European System G (C.C.I.R. designations).

Fig. 10 shows the transfer characteristics of the a.f.c. discriminator for a $50k\Omega$ load.

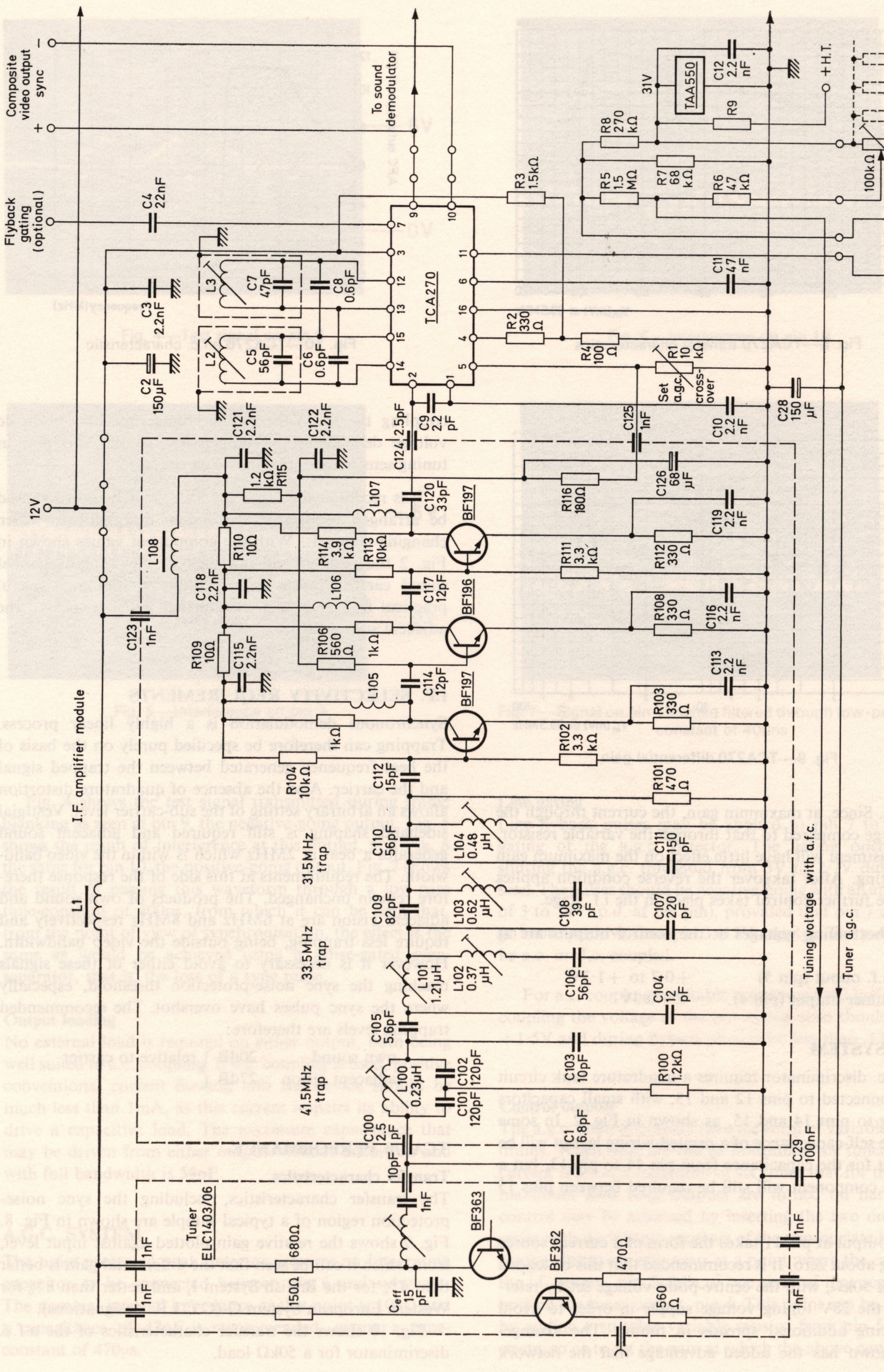
Composite video output sync
Flyback gating (optional)
To sound demodulator
TCA270
TAA550
31V
+H.T.
100kΩ Tuning pots
a.f.c. switch
Set a.g.c. cross-over
12V
I.F. amplifier module
BF197
BF196
BF197
31.5MHz trap
33.5MHz trap
41.5MHz trap
Tuner ELC1403/06
BF363
BF362
Tuning voltage with a.f.c.
Tuner a.g.c.
337/118

Fig. 11a—Tuner, i.f. amplifier and demodulator circuit using TCA270. (Continued in Fig 11b)

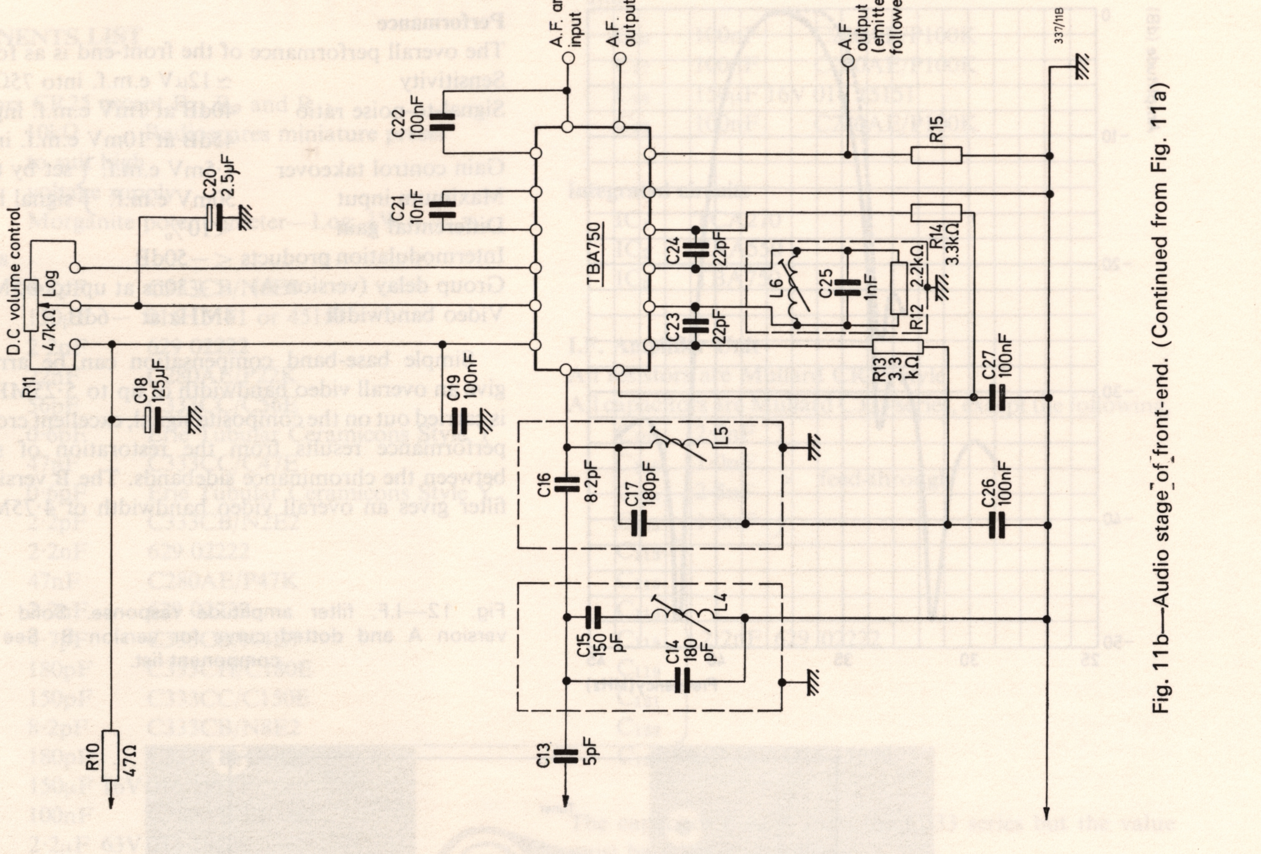
A.F. amp input
A.F. output
A.F. output (emitter follower)
TBA750
D.C. volume control
R11 47kΩ Log
337/118

Fig. 11b—Audio stage of front-end. (Continued from Fig. 11a)

Intermodulation products

The 1·6 and 2·9MHz intermodulation products measured with a signal spectrum corresponding to the 95% blue colour bar are quoted below for a full carrier level of 70mV. Allowance is made for vestigial sideband shaping and sound carrier trapping of 20dB relative to vision carrier.

Signal levels:

Carrier	39·5MHz	−4·7dB
Sub-carrier	35·1MHz	−14·5dB
Sound carrier	33·5MHz	−27dB

Intermodulation products, r.m.s. with respect to black-to-white:

Typically	1·6MHz	−60dB
	2·9MHz	−67dB

Video bandwidth

The video bandwidth of the TCA270 is typically 5MHz at −3dB

TV RECEIVER FRONT-END

The TCA270 has been incorporated in a television receiver front-end, the circuit diagram of which is shown in Fig. 11. The demodulator is fed from a three-stage amplifier with fixed-tuned, wideband L/C coupling giving a bandwidth of approximately 8.5MHz centred on 37MHz. The second stage is gain controlled, giving a good compromise between signal-to-noise ratio and signal-handling. The sensitivity at the amplifier input is 25μV.

The main selectivity is provided by a filter coupling the ELC1043/06 tuner to the i.f. input. This is a computed linear-phase design and requires only six adjustments including the usual traps at 31·5, 33·5 and 41·5MHz. The response curve of the filter is shown in Fig. 12 which also shows the response of a modified version, B. This version has capacitor C106 (Fig. 11) changed to 33pF, and gives increased bandwidth at the expense of h.f. group-delay. Both filters are designed for use with the ELC1043/06 tuner as some of the tuner components are part of the filter design.

Since the amplifier includes little selectivity it is necessary to screen not only the filter but also at least the input stage, in order to avoid picking up interference from such sources as channel 1 sound carrier. In the laboratory the entire filter and amplifier were built into a metal box similar to that used for the tuner.

A typical layout is shown in Fig. 13. This represents an actual board from a laboratory model: such boards are not supplied by Mullard Ltd. and the drawing is included merely to indicate one usable layout. The component references in Fig. 13 relate to the circuit in Fig. 11.

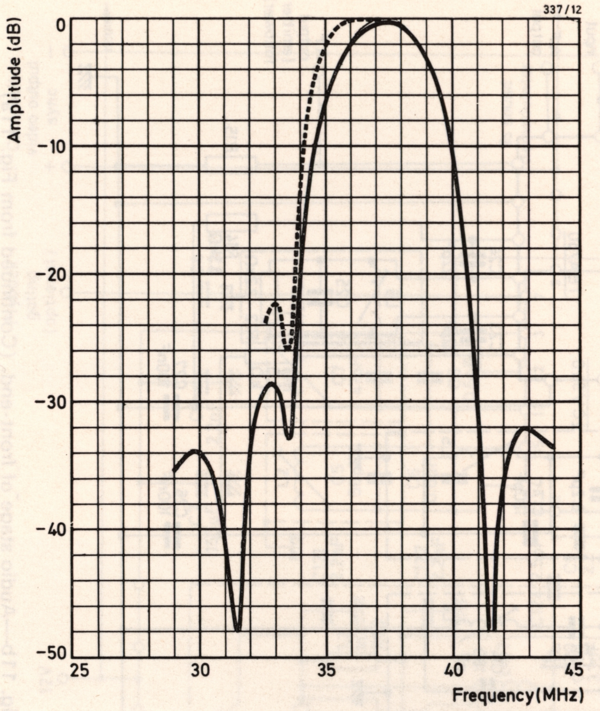

Fig. 12—I.F. filter amplitude response. Solid curve for version A and dotted curve for version B. See text and component list.

Performance

The overall performance of the front-end is as follows:

Sensitivity	≃12μV e.m.f. into 75Ω	
Signal-to-noise ratio	40dB at 1mV e.m.f. input 45dB at 10mV e.m.f. input	
Gain control takeover	1·5mV e.m.f.	set by tuner signal handling
Maximum input	50mV e.m.f.	
Differential gain	<10%	
Intermodulation products	<−50dB	
Group delay (version A)	<±30ns at up to 4·5MHz	
Video bandwidth	4MHz at −6dB	

Simple base-band compensation can be arranged to give an overall video bandwidth of up to 5·25MHz. If this is carried out on the composite signal, excellent cross-colour performance results from the restoration of symmetry between the chrominance sidebands. The B version of the filter gives an overall video bandwidth of 4·75MHz.

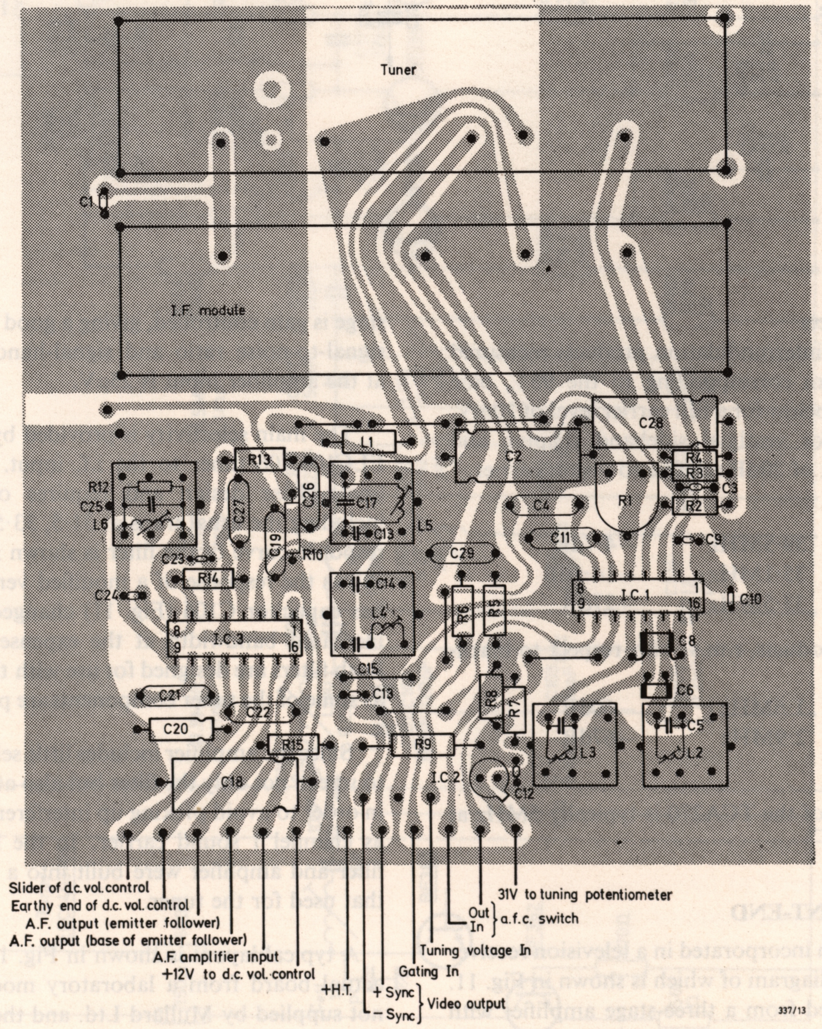
Tuner
I.F. module
C1
L1
C28
R13
C26
C17
L5
C2
C4
R1
C11
C9
C10
C29
I.C.1
C8
C6
C5
L2
L3
L4
R12
C25
L6
C27
C19
R10
C13
C23
C24
R14
I.C.3
C14
C15
C21
C22
C20
R15
R9
C18
I.C.2
C12
R6
R8
R7
R3
R2
R4
Slider of d.c. vol. control
Earthy end of d.c. vol. control
A.F. output (emitter follower)
A.F. output (base of emitter follower)
A.F. amplifier input
+12V to d.c. vol. control
+H.T.
+ Sync
− Sync
Video output
Gating In
Tuning voltage In
Out
In
a.f.c. switch
31V to tuning potentiometer
337/13

Fig. 13—Typical layout board for front-end using TCA270
(These boards are not supplied by Mullard Ltd.)

COMPONENTS LIST

Resistors

All resistors CR25 except R_1, R_9 and R_{11}.

R_1	10kΩ	Radiospares miniature preset
R_9	to suit high voltage supply	
R_{11}	Morganite potentiometer—Log. ¼W	

Capacitors

C_1	6·8pF	C333CB/N6E8
C_2	150μF	016 15151 or 45151
C_3	2·2nF	629 02222
C_4	22nF	C280AE/P22K
C_5	56pF	C333CC/C56E
C_6	0·6pF	Erie Tubular Ceramicons Style Y
C_7	47pF	C333CC/C47E
C_8	0·6pF	Erie Tubular Ceramicons Style Y
C_9	2·2pF	C333CB/N2E2
C_{10}	2·2nF	629 02222
C_{11}	47nF	C280AE/P47K
C_{12}	2·2nF	629 02222
C_{13}	4·7pF	C333CB/N4E7
C_{14}	180pF	C333CH/C180E
C_{15}	150pF	C333CC/C150E
C_{16}	8·2pF	C333CB/N8E2
C_{17}	180pF	C333CH/C180E
C_{18}	150μF 16V	016 15151
C_{19}	100nF	C280AE/P100K
C_{20}	2·2μF 63V	015 18228
C_{21}	10nF	C280AE/P10K
C_{22}	100nF	C280AE/P100K
C_{23}	22pF	C333CC/C22E
C_{24}	22pF	C333CC/C22E
C_{25}	1nF	Suflex polystyrene type Hs
C_{26}	100nF	C280AE/P100K
C_{27}	100nF	C280AE/P100K
C_{28}	150μF 16V	016 15151
C_{29}	100nF	C280AE/P100K

Integrated circuits

IC_1	TCA270
IC_2	TAA550
IC_3	TBA750

I.F. Amplifier Unit

All resistors are Mullard CR25 style

All capacitors are Mullard C333 series, except the following,

C_{100}	2·5nF	feed-through
C_{123}	1·0nF	
C_{124}	2·5nF	
C_{125}	1·0nF	
C_{113} C_{115} C_{116} C_{118} C_{119} C_{121} C_{122}	2·2nF	629 02222
C_{126}	68μF 16V	O16 15689

The capacitor C_{106} is from the C333 series but the value must be selected as follows,

C_{106}	A	56pF	(See L_{102})
	B	33pF	

Transistors BF196, 2×BF197

Inductors

Coil		Winding	Core
L_1, L_2		Max. no. of turns 0·1mm (42 swg) en. cu.	Neosid choke core CH2/1/500
L_3, L_4		7 turns, 0·45mm (26 swg) t.n.a.	Neosid core 4×0·5×6/900
L_5		48 turns, 42 swg, t.n.a.	E.I.H. type P1011 19mm (0·75in) former E.I.H. type P1001 12·5×12·5mm (0·5×0·5in) base E.I.H. type P5000 19·0×12·5×12·5mm (0·75×0·5×0·5in) can
L_6		30 turns, 42 swg, t.n.a.	
L_7		10 turns, 30 swg, t.n.a.	
L_{100}		5 turns, 30 swg, t.n.a.	
L_{101}		15 turns, 30 swg, t.n.a.	
L_{102}	A	7 turns, 30 swg, t.n.a.	
	B	10 turns, 30 swg, t.n.a.	
L_{103}		10 turns, 30 swg, t.n.a.	
L_{104}		7 turns, 30 swg, t.n.a.	
L_{105} L_{106} L_{107}		23 turns, 0·1mm (42 swg) t.n.a.	CR25 resistor with sleeving

Note: Double silk covered wire can be used to replace t.n.a.

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